NEHRU COLLEGE OF ENGINEERING AND RESEARCH CENTRE
(NAAC Accredited)
(Approved by AICTE, Affiliated to APJ Abdul Kalam Technological University, Kerala)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE MATERIALS

ECL 331: ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2002
- Course offered: B.Tech in Electronics and Communication Engineering

  M.Tech in VLSI
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

DEPARTMENT VISION

Providing Universal Communicative Electronics Engineers with corporate and social relevance towards sustainable developments through quality education.

DEPARTMENT MISSION

1) Imparting Quality education by providing excellent teaching, learning environment.

2) Transforming and adopting students in this knowledgeable era, where the electronic gadgets (things) are getting obsolete in short span.

3) To initiate multi-disciplinary activities to students at earliest and apply in their respective fields of interest later.

4) Promoting leading edge Research & Development through collaboration with academia & industry.

PROGRAMME EDUCATIONAL OBJECTIVES

PEOI. To prepare students to excel in postgraduate programmes or to succeed in industry / technical profession through global, rigorous education and prepare the students to practice and innovate recent fields in the specified program/ industry environment.

PEO2. To provide students with a solid foundation in mathematical, Scientific and engineering fundamentals required to solve engineering problems and to have strong practical knowledge required to design and test the system.

PEO3. To train students with good scientific and engineering breadth so as to comprehend, analyze, design, and create novel products and solutions for the real-life problems.

PEO4. To provide student with an academic environment aware of excellence, effective communication skills, leadership, multidisciplinary approach, written ethical codes and the life-long learning needed for a successful professional career.

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Ability to Formulate and Simulate Innovative Ideas to provide software solutions for Real-time Problems and to investigate for its future scope.

PSO2: Ability to learn and apply various methodologies for facilitating development of

high quality
System Software Tools and Efficient Web Design Models with a focus on performance optimization.

PSO3: Ability to inculcate the Knowledge for developing Codes and integrating hardware/software
products in the domains of Big Data Analytics, Web Applications and Mobile Apps to create innovative career path and for the socially relevant issues.

SYLLABUS

ECL331	ANALOG INTEGRATED CIRCUITS AND SIMULATION LAB	CATEGORY	L	T	P	CREDIT
		PCC	0	0	3	2

Preamble: This course aims to (i) familiarize students with the Analog Integrated Circuits and Design and implementation of application circuits using basic Analog Integrated Circuits (ii) familiarize students with simulation of basic Analog Integrated Circuits.

Prerequisite: ECL202 Analog Circuits and Simulation Lab

Course Outcomes: After the completion of the course the student will be able to

CO 1	Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs.
CO 2	Design and simulate the application circuits with Analog Integrated Circuits using simulation tools.
CO 3	Function effectively as an individual and in a team to accomplish the given task.

Mapping of course outcomes with program outcomes

	PO1	PO 2	PO3	PO 4	PO5	PO 6	PO7	PO8	PO9	PO 10	PO 11	PO 12
CO1	3	3	3						2			2
CO2	3	3	3	2	3				2			2
CO3	2	2	2		2				3	2		3

Assessment
Mark distribution

Total Marks	CIE	ESE	ESE Duration
150	75	75	3 hours

Continuous Evaluation Pattern

Attendance : 15 marks
Continuous Assessment : 30 marks
Internal Test (Immediately before the second series test) : 30 marks

End Semester Examination Pattern: The following guidelines should be followed regarding awardof marks

(a) Preliminary work : 15 Marks
(b) Implementing the work/Conducting the experiment : 10 Marks
(c) Performance, result and inference (usage of equipments and trouble shooting): 25 Marks
(d) Viva voce : 20 marks
(e) Record : 5 Marks

General instructions: End-semester practical examination is to be conducted immediately after the second series test covering entire syllabus given below. Evaluation is to be conducted under the equal responsibility of both the internal and external examiners. The number of candidates evaluated per day should not exceed 20. Students shall be allowed for the examination only on submitting the duly certified record. The external examiner shall endorse the record.

Course Level Assessment Questions (Examples only)

Course Outcome 1 (CO1): Use data sheets of basic Analog Integrated Circuits and design and implement application circuits using Analog ICs.

1. Measure important opamp parameters of µA 741 and compare them with the data provided in the data sheet
2. Design and implement a variable timer circuit using opamp
3. Design and implement a filter circuit to eliminate 50 Hz power line noise.

Course Outcome 2 and 3 (CO2 and CO3): Design and simulate the application circuits with Analog Integrated Circuits using simulation tools.

1. Design a precission rectifier circuit using opamps and simulste it using SPICE
2. Design and simulate a counter ramp ADC

List of Experiments

I. Fundamentals of operational amplifiers and basic circuits [Minimum seven experiments are to be done]

1. Familiarization of Operational amplifiers - Inverting and Non inverting amplifiers, frequency response, Adder, Integrator, Comparators.
2. Measurement of Op-Amp parameters.
3. Difference Amplifier and Instrumentation amplifier.
4. Schmitt trigger circuit using Op–Amps.
5. Astable and Monostable multivibrator using Op-Amps.
6. Waveform generators using Op-Amps - Triangular and saw tooth
7. Wien bridge oscillator using Op-Amp - without & with amplitude stabilization.

8. RC Phase shift Oscillator.
9. Active second order filters using Op-Amp (LPF, HPF, BPF and BSF).
10. Notch filters to eliminate the 50Hz power line frequency.
11. Precision rectifiers using Op-Amp.

II. Application circuits of **555 Timer/565 PLL/ Regulator(IC 723) ICs** [Minimum three experiments are to be done]

1. Astable and Monostable multivibrator using Timer IC NE555
2. DC power supply using IC 723: Low voltage and high voltage configurations, Short circuit and Fold-back protection.
3. A/D converters- counter ramp and flash type.
4. D/A Converters - R-2R ladder circuit
5. Study of PLL IC: free running frequency lock range capture range

III. Simulation experiments [The experiments shall be conducted using SPICE]

1. Simulation of any three circuits from Experiments 3, 5, 6, 7, 8, 9, 10 and 11 of section I
2. Simulation of Experiments 3 or 4 from section II

Textbooks

1. D. Roy Choudhary, Shail B Jain, "Linear Integrated Circuits,"
2. M. H. Rashid, "Introduction to Pspice Using Orcad for Circuits and Electronics", Prentice Hall

PREPARATION FOR THE LABORATORY SESSION
GENERAL INSTRUCTIONS TO STUDENTS

1. Read carefully and understand the description of the experiment in the lab manual. You may go to the lab at an earlier date to look at the experimental facility and understand it better. Consult the appropriate references to be completely familiar with the concepts and hardware.

2. Make sure that your observation for previous week experiment is evaluated by the faculty member and you have transferred all the contents to your record before entering to the lab/workshop.

3. At the beginning of the class, if the faculty or the instructor finds that a student is not adequately prepared, they will be marked as absent and not be allowed to perform the experiment.

4. Bring necessary material needed (writing materials, graphs, calculators, etc.) to perform the required preliminary analysis. It is a good idea to do sample calculations and as much of the analysis as possible during the session. Faculty help will be available. Errors in the procedure may thus be easily detected and rectified.

5. Please actively participate in class and don't hesitate to ask questions. Please utilize the teaching assistants fully. To encourage you to be prepared and to read the lab manual before coming to the laboratory, unannounced questions may be asked at any time during the lab.

6. Carelessness in personal conduct or in handling equipment may result in serious injury to the individual or the equipment. Do not run near moving machinery/equipment. Always be on the alert for strange sounds. Guard against entangling clothes in moving parts of machinery.

7. Students must follow the proper dress code inside the laboratory. To protect clothing from dirt, wear a lab coat. Long hair should be tied back. Shoes covering the whole foot will have to be worn.

8. In performing the experiments, please proceed carefully to minimize any water spills, especially on the electric circuits and wire.

9. Maintain silence, order and discipline inside the lab. Don't use cell phones inside the laboratory.

10. Any injury no matter how small must be reported to the instructor immediately.

11. Check with faculty members one week before the experiment to make sure that you have the handout for that experiment and all the apparatus.

AFTER THE LABORATORY SESSION

1. Clean up your work area.

2. Check with the technician before you leave.

3. Make sure you understand what kind of report is to be prepared and due submission of record is next lab class.

4. Do sample calculations and some preliminary work to verify that the experiment was successful

MAKE-UPS AND LATE WORK

Students must participate in all laboratory exercises as scheduled. They must obtain permission from the faculty member for absence, which would be granted only under justifiable circumstances. In such an event, a student must make arrangements for a make-up laboratory, which will be scheduled when the time is available after completing one cycle. Late submission will be awarded less mark for record and internals and zero in worst cases.

LABORATORY POLICIES

1. Food, beverages & mobile phones are not allowed in the laboratory at any time.

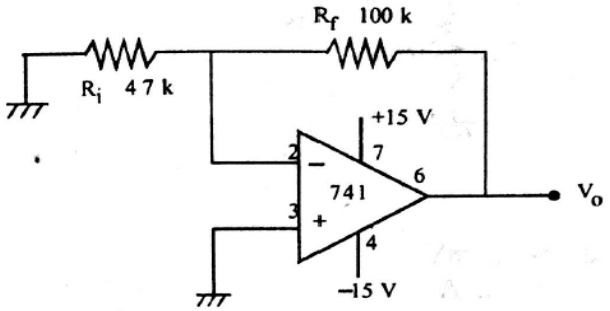
2. Do not sit or place anything on instrument benches.

3. Organizing laboratory experiments requires the help of laboratory technicians and staff. Be punctual.

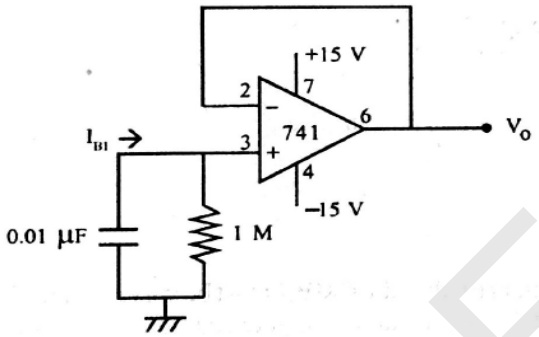
INDEX

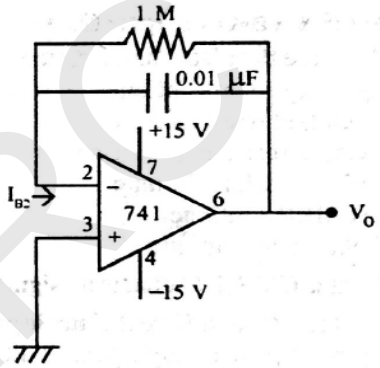
Circuit diagram

To measure input offset voltage

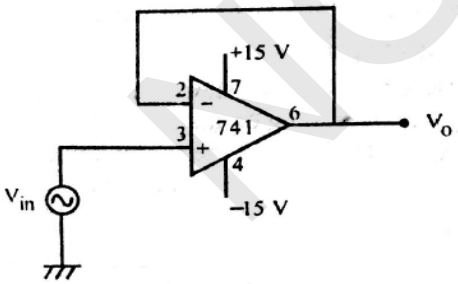


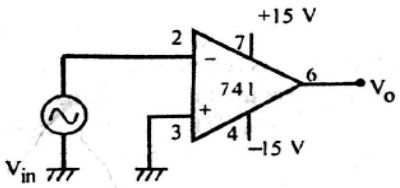
To measure input bias and input offset currents



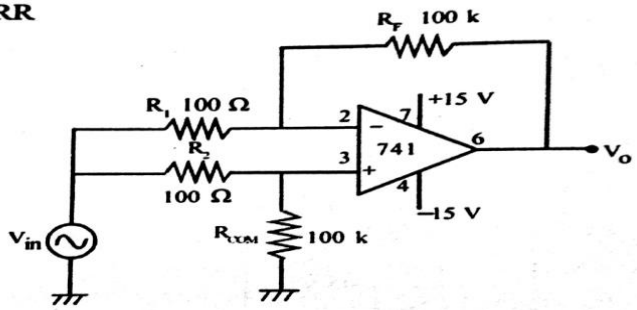


To measure slew rate





CMRR



Exp No: 1 **Date:**

MEASUREMENT OF OP-AMP PARAMETERS

AIM:

To measure the following parameters of an Op-amp i.e, input bias current, input offset voltage, input offset current, CMRR and slew rate.

APPARATUS REQUIRED:

The following components and equipments are used to measure the op-amp parameters

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	4.7KΩ,100KΩ (2), 1MΩ, 100Ω (2),	Each one
5	Capacitor	0.01μF	1
6	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Input bias current I_B: It is defined as the average of the currents entering into the inverting and non-inverting terminals of an op-amp. $I_B=(I_{b1}+I_{b2})/2$. Typical value of input bias current is 80nA.

Input bias current I_O: It is defined as the algebraic difference between the currents entering into the inverting and non-inverting terminals of an op-amp. $I_O=|I_{b1}+I_{b2}|$. Typical value of input offset current is 20nA.

Input offset voltage: It is defined as the small voltage which is applied to overcome circuit imbalances due to which the output voltage is not zero for zero input voltage, ie voltage applied between the input terminals of an op-amp to nullify the output voltage. Typical value of input offset voltage is 2mV.

CMRR: It is the ratio of differential mode gain to common mode gain and is expressed in dB. CMRR=20 log (A_d/A_c) in dB.

Slew rate: It is the rate of rise of output voltage. It is a measure of fastness of op-amp. It is expressed in v/μs.

PROCEDURE:

1. Set up the circuit to find the input offset voltage.

2. Measure the output voltage using the expression, $V_{iO}=V_O R_i/(R_f + R_i)$; where V_O is the output voltage and V_{iO} is the input offset voltage..
3. Set up the circuits for measuring input bias current and input bias voltage
4. Measure the output voltage using the expressions $V_O= I_{b1}R$ and $V_O= I_{b2}R$.
5. Calculate I_{B1} and I_{B2} and measure the bias and offset currents using the expression $I_B=(I_{b1}+I_{b2})/2$and $I_O=|I_{b1}+I_{b2}|$. Where I_B is bias current, I_O is offset current.
6. Setup the circuit to calculate the slew rate. Give a square input of 1 $V_{pp,}$ 1kHz. Vary the input frequency and observe the output. Note down the frequency at which the output gets disturbed. Calculate the slew rate using the expression $SR=(2\pi fV_m)/10^6$
7. Set up the circuits for finding CMRR and apply a dc signal of 0.5v to input and measure V_O. Calculate the CMRR using the expression $CMRR=V_i(R_f/R_i)/V_O$. Express the CMRR in dB using the expression 20 log(CMRR).

RESULT:

The various op-amp parameters were measured experimentally.

INFERENCE:

Input offset voltage = ……..mV
Input bias current = ……..A
Input offset current = ...…...A
Slew rate = ……..V/μs.
CMRR = …….dB

VIVA QUESTIONS:

1. State the ideal characteristics of Op-amp.

i) Open loop gain = ∞
ii) Input impedance, Ri = ∞
iii) Output Impedance, Ro = 0
iv) Zero Offset, Vo = 0
v) Bandwidth, BW = ∞
vi) Slew rate = ∞
vii) CMRR = ∞

2. Why differential amplifier is used as an input stage of IC op-amp?

The differential amplifier eliminates the need for an emitter bye-pass capacitor. So, differential amplifier is used as an input stage in op-amp ICs.

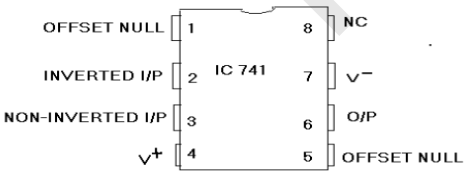
3. What does operational amplifier refers to?

Operational amplifier refers to an amplifier that performs a mathematical operation. A typical op-amp is a DC amplifier with a very high voltage gain, very high input impedance and very low output impedance.

4. What causes slew rate?

The rate at which internal or external capacitance of Op-amp changes causes slew rate. Also slew rate is caused by current limiting and saturation of internal stages of op-amp where a high frequency, large – amplitude signal is applied.

5. Draw the Pin diagram of IC 741.



6. What is input bias current?

The average of the currents entering the negative input and positive input of an op-amp is called input bias current.

7. Why do we use Rcomp resistor?

In a bipolar op-amp circuit, even when the input is zero, the output will not be zero. This is due to effect of input bias current. This effect can be compensated by using compensation resistor Rcomp.

8. What is thermal drift?

In an op-amp the bias current, offset current and off set voltage changes with change in temperature. Offset current drift is measured in nA/ 0C and offset voltage drift is measured in mV/ 0C. These indicate the change in offset current or voltage for each degree Celsius change in temperature. Forced air cooling may be used to stabilize the ambient temperature.

9. Why is IC741 op-amp not used for high frequency applications?

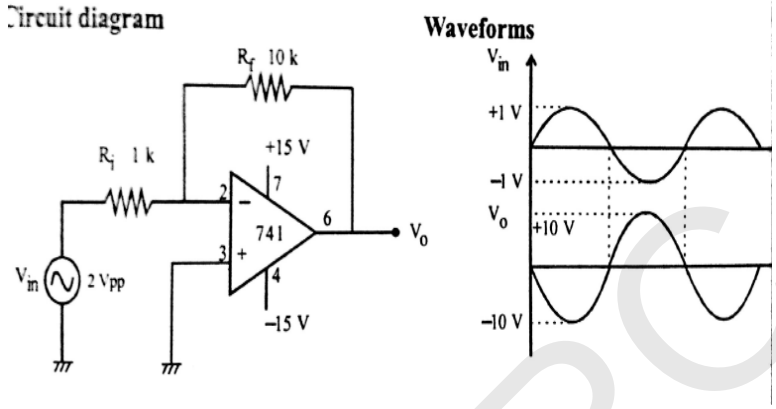
Op-amp IC741 has very low slew rate (0.5V/μS) and therefore cannot be used for high frequency applications.

10. What is unity gain circuit?

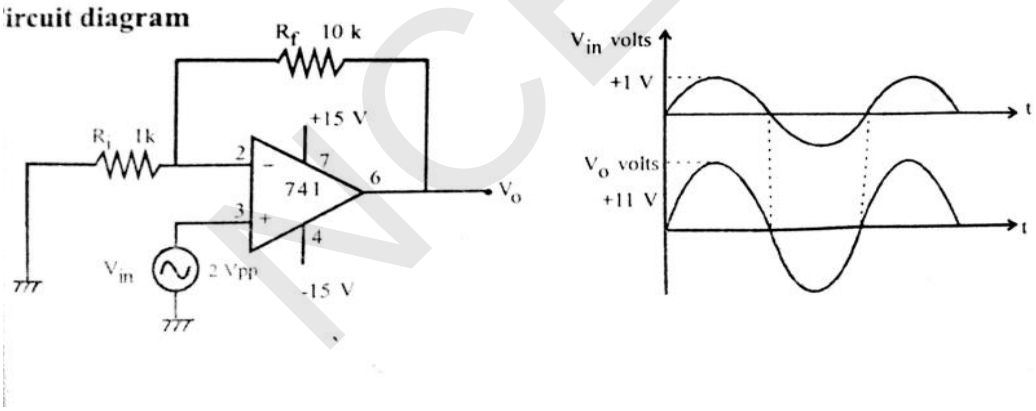
Voltage follower is called unity gain circuit. The circuit does not amplify and provides constant gain of unity.

CIRCUIT DIAGRAMS:

INVERTING AMPLIFIER



NON-INVERTING AMPLIFIER



DESIGN:

Inverting amplifier:

$A = -Rf/R1$

Take $A = 10$

Let $R1 = 1\ k\Omega$

Then $Rf = 10k\Omega$

Non inverting amplifier:

$A = 1 + Rf/R1$

Take $A = 11$

$R1 = 1\ k\Omega$

Then $Rf = 10k\Omega$

Exp No:2.1 **Date:**

INVERTING AND NON-INVERTING AMPLIFIERS

AIM:

To design and set up an inverting and non- inverting amplifier.

APPARATUS REQUIRED:

The following components and equipments are used to set up amplifiers.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	10KΩ,1KΩ	Each one
5	Op-amp	IC 741	1
6	Bread board	-	1
7	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Inverting amplifier: This is the most widely used op-amp. Here, the output voltage Vo is feedback to the inverting input terminal through the Rf – R1 network. The negative sign in gain indicates the phase shift of 180^o.

Non inverting amplifier: If signal is applied to the non-inverting input terminal of op-amp without inverting the input signal such a circuit is called non-inverting amplifier. Here the output is feedback to the inverting input terminal. The phase shift of input signal does not occur in non-inverting terminal.

PROCEDURE:

1. Set up the inverting amplifier on the bread board.
2. Feed a $2V_{pp}$ sine wave and observe the input and output simultaneously on CRO. Verify whether the output is $22V_{pp}$ sine wave in phase with input.
3. Set up the non inverting amplifier on the bread board.
2. Feed a $2V_{pp}$ sine wave and observe the input and output simultaneously on CRO. Verify whether the output is $20V_{pp}$ sine wave with 180^0 out of phase with input.

RESULT:

Inverting and non inverting amplifiers were designed and studied.

INFERENCE:

Inverting amplifier: Input voltage =……
Output voltage =……
Gain of the amplifier =……...
Non-inverting amplifier: Input voltage =……
Output voltage =……
Gain of the amplifier =……...

VIVA QUESTIONS:

1. Mention some of the linear applications of op – amps:

Adder, subtractor, voltage –to- current converter, current –to- voltage converters, instrumentation amplifier, analog computation, power amplifier, etc are some of the
linear op-amp circuits.

2. Mention some of the non – linear applications of op-amps:

Rectifier, peak detector, clipper, clamper, sample and hold circuit, log amplifier, anti –log amplifier, multiplier are some of the non – linear op-amp circuits.

3. What are the areas of application of non-linear op- amp circuits:

- Industrial instrumentation
- Signal processing

4. What does 74LS refers to:

74-refers to IC which can be used for commercial purpose.LS-Low Power Schottky.

5. What is Linear IC?

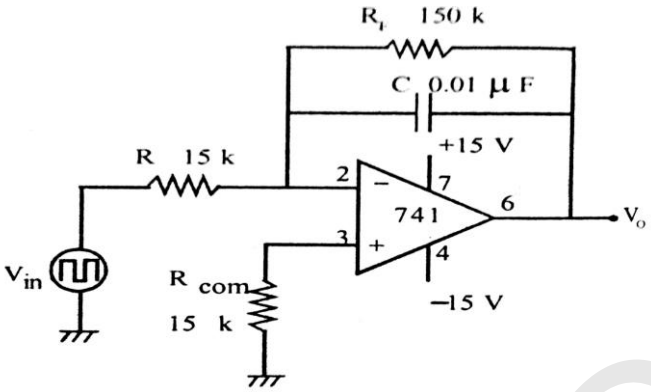
IC which accepts, process and produce analog signal is called linear IC. Eg: IC741, IC555.

6.What is gain of the inverting amplifier?

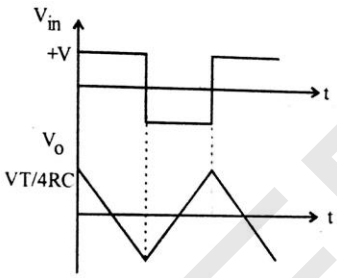
A= - Rf / Ri

CIRCUIT DIAGRAMS:

INTEGRATOR



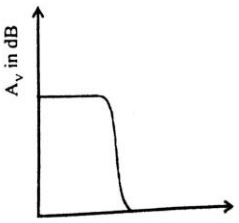
Waveforms



Tabular column

f in Hz	V_o	log (f)	A_V in dB

Frequency response



DESIGN:

INTEGRATOR:

Let input frequency be ,f= 1 kHz

$f = 1/ (2\pi RC)$

Take C=0.01 μf. Then R=15.9. Use 15k std.

Select $R_f = 10$ R = 10 * 15 k = 150 k so that break frequency is 100 Hz.

Select R_{com} = 15k

Exp No: 2.2 **Date:**

INTEGRATOR AND DIFFERENTIATOR

AIM:

To design and set up integrator and differentiator circuits using op-amp and plot their frequency responses.

APPARATUS REQUIRED:

The following components and equipments are used to design and set up integrator and differentiator

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	150KΩ, 15KΩ(2), 5.6KΩ(2)	Each one
5	Capacitors	0.01uf, 0.1uf(2)	1
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Integrator: In an integrator circuit, the output voltage is integral of the input signal. The output voltage of an integrator is given by

$$V_o = -1/R_1C_f \int_o^t Vidt$$

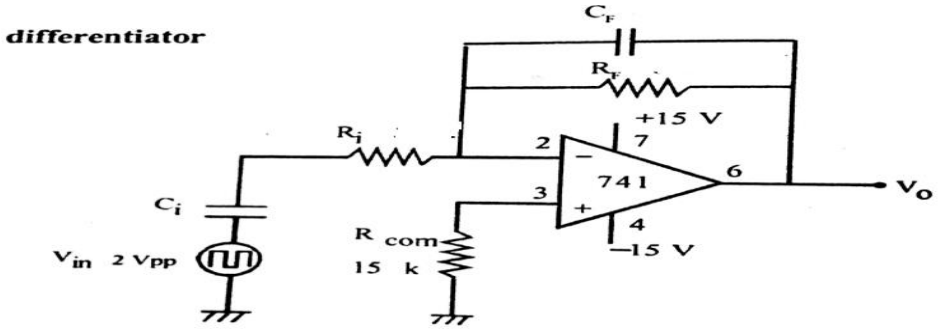
At low frequencies the gain becomes infinite, so the capacitor is fully charged and behaves like an open circuit. The gain of an integrator at low frequency can be limited by connecting a resistor in shunt with capacitor.

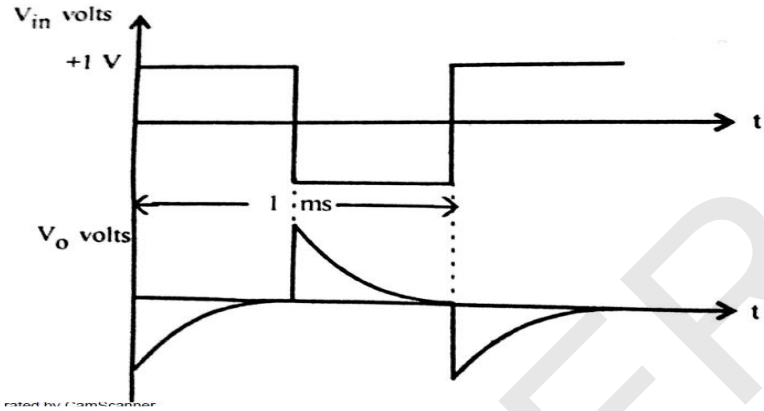
Differentiator: In the differentiator circuit the output voltage is the differentiation of the input voltage. The output voltage of a differentiator is given by

$$V_o = -RfC_1 \frac{dV_i}{dt}$$

The input impedance of this circuit decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise. At high frequencies circuit may become unstable.

DIFFERENTIATOR:





DESIGN:

DIFFERENTIATOR:

Frequency at which gain become zero dB $f_a = 1/(2\pi R_f C_f) = 1$ kHz
Let $C_f = 0.01$uF, Then $R_f = 15.9$k. Use 15k std.
Let Gain limiting frequency, $f_b = 1/(2\pi R_f C_f) = 10 f_a = 10$kHz
Take $C_i = 0.01$uF, Then $R_i = 1.59$k. Use 1.5k std.
Select $R_{com} = 15$k

PROCEDURE:

INTEGRATOR:

1. Set up the integrator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response.

DIFFERENTIATOR:

1. Set up the differentiator circuit.
2. Feed 1V, 1ms square wave at the input and observe the input and output simultaneously on CRO.
3. Feed a sine wave to the input and note down the output amplitude by varying the frequency of the sine wave. Enter it in tabular column and plot the frequency response

RESULT:

Integrator and differentiator circuits were studied and plotted their frequency responses.

INFERENCE:

Cut off frequency of low pass filter =:…….Hz
Frequency at which gain become zero dB in differentiator=:……Hz
Gain limiting frequency of differentiator =:……Hz

VIVA QUESTIONS:

1.What are the limitations of the basic differentiator circuit:

At high frequency, a differentiator may become unstable and break into oscillations. The input impedance decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

2.Write down the condition for good differentiation: -

For good differentiation, the time period of the input signal must be greater than or equal to $R_f C_1$, $T > R_f C_1$ Where, R_f is the feedback resistance

3.What is an IC:

The term IC refers to complex electronic circuits consisting of a large number of components on a single substrate.

4.What are the advantage of IC:

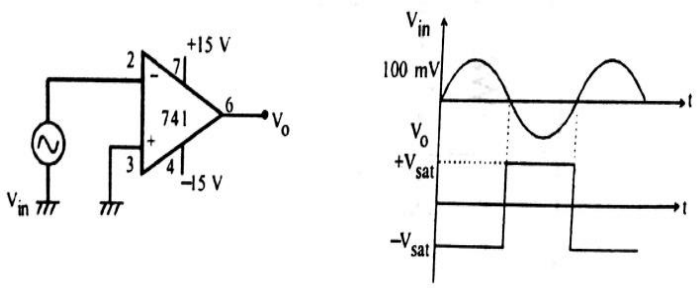
Cost reduction, increased operating speed, reduced power consumption and improved functional performance.

5.What are the different IC technologies:

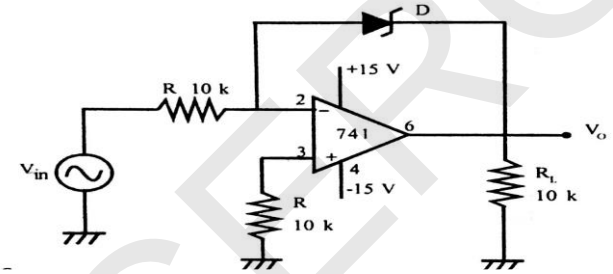
Monolithic technology and Hybrid technology

CIRCUIT DIAGRAMS:

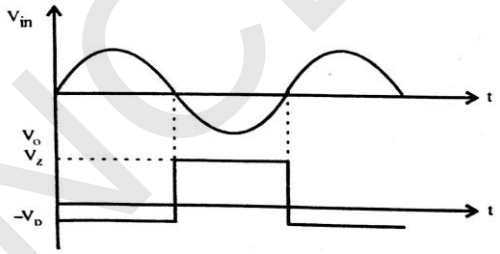
ZERO CROSSING DETECTOR



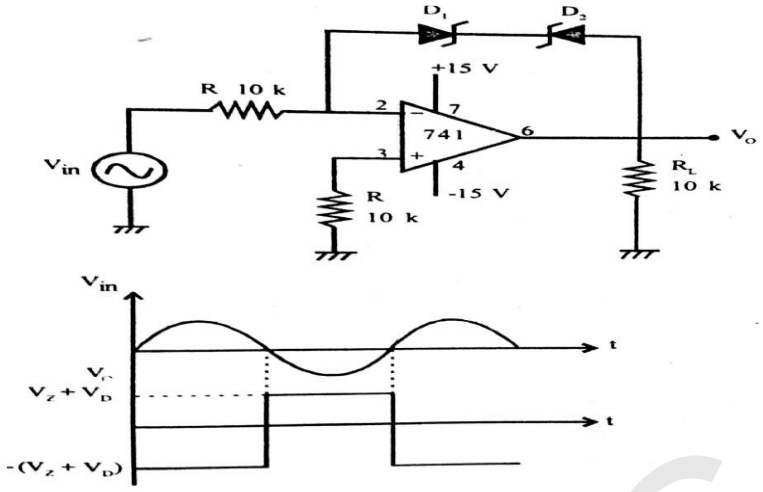
VOLTAGE LIMITER 1



Waveform



VOLTAGE LIMITER 2



Exp No:2.3 **Date:**

COMPARATOR CIRCUITS

AIM:

To design and set up the following comparator circuits:

1. Zero Crossing Detector
2. Voltage limiter
3. Schmitt trigger

APPARATUS REQUIRED:

The following components and equipments are used for comparator circuits.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	22KΩ, 10KΩ(2), 3.3KΩ, 1KΩ	Each one
5	Zener diodes	Sz5.6	2
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Zero crossing detector: It is a comparator that switches output from off to on. The output is given into negative saturation when the input signal passes through zero in the positive direction and vice versa. When the input signal passes through zero in negative direction the output switches into positive saturation.

Voltage Limitter: They are zero crossing detectors with output limited to pre determined levels.

PROCEDURE:

1. Verify whether the op-amp was in good condition.
2. Set up the Zero crossing detector on the bread board and feed a 100mV sine wave at the input and verify whether the output is a square wave swinging from +13V to -13V.
3. **RESULT:**

Comparator circuits were designed and studied.

INFERENCE:

Voltage levels:

Zero crossing detector =……

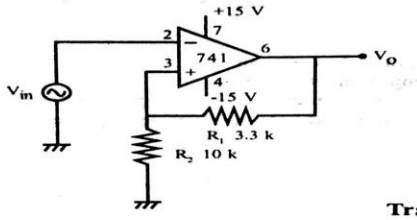
Voltage limiter 1 =……

Voltage limiter 2 =……

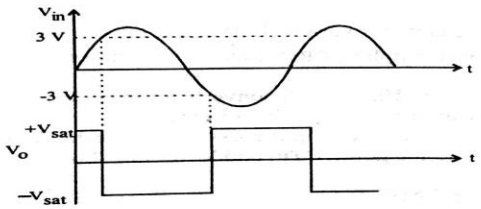
SCHMITT TRIGGER 1:

Circuit diagram

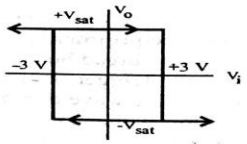
Schmitt trigger for LTP = -3 V and UTP = 3 V



Waveforms



Transfer characteristics



DESIGN:

Let the required LTP be – 3 V and a UTP be +3 V.

Normally, V_{sat} = 13 V when V = 15 V

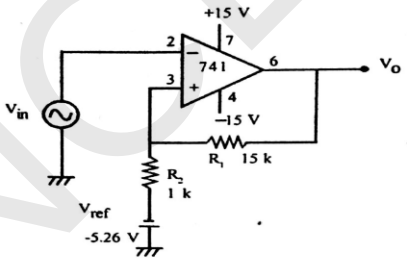
LTP = – 3 V = $-13R_2/(R_1 + R_2)$

UTP = 3 V = $13R_2/(R_1 + R_2)$

Take R_2 = 3.3 k and R_1 = 10 k.

SCHMITT TRIGGER 2 :

Schmitt Trtigger for a LTP = -6 V and UTP = -4 V



Design

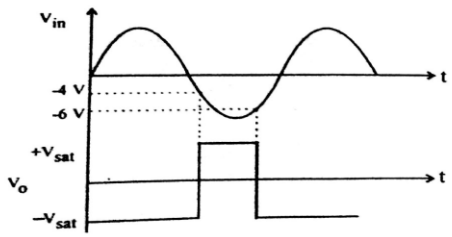
LTP = $-6\text{ V} = -15R_2/(R_1 + R_2) + V_{ref}R_1/(R_1 + R_2)$ .....(2)

UTP = $-4\text{ V} = 15R_2/(R_1 + R_2) + V_{ref}R_1/(R_1 + R_2)$ .....(1)

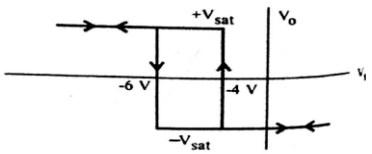
Take R_2 = 1 k. Then and R_1 = 15 k.

Vref = -5.26 V.

Waveforms



Transfer characteristics



Exp No:3 **Date:**

SCHMITT TRIGGER

To design and set up the following Schmitt trigger circuits:

APPARATUS REQUIRED:
The following components and equipment are used for comparator circuits.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	22KΩ, 10KΩ(2), 3.3KΩ, 1KΩ	Each one
5	Zener diodes	Sz5.6	2
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Schmitt Trigger: Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform. The circuit connects an irregular shaped wave form to a square wave or pulse form. It is also known as a squaring circuit.

1. Verify whether the op-amp was in good condition.
2. Set up the circuit for Schmitt trigger and switch on the supplies and observe the input and output on the CRO screen.

RESULT:

Comparator circuits were designed and studied.

INFERENCE:

Voltage levels:

Zero crossing detector =……
Voltage limiter 1 =……
Voltage limiter 2 =…….
Schmitt trigger 1 , LTP =…… and UTP =……..
Schmitt trigger 2 , LTP =…… and UTP =…….

VIVA QUESTIONS:

1.What are the applications of comparator?

Zero crossing detectors
Window detector
Time marker generator
Phase detector

2. What is a Schmitt trigger?

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform.

3.What is the other name for Schmitt trigger circuit?

Regenerative comparator

4.In Schmitt trigger which type of feedback is used?

Positive feedback.

5.What is meant by hysteresis?

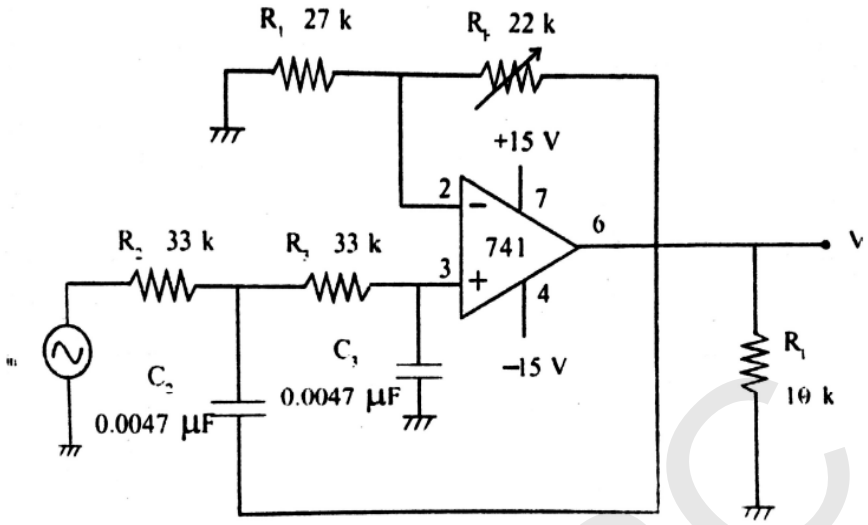
The comparator with positive feedback is said to be exhibit hysteresis, a deadband condition. When the input of the comparator is exceeds V_{utp}, its output switches from $+V_{sat}$ to $-V_{sat}$ and reverts back to its original state,$+V_{sat}$,when the input goes below $V_{ltp.}$

6.What are effects of input signal amplitude and frequency on output?

The input voltage triggers the output every time it exceeds certain voltage levels (UTP and LTP). Output signal frequency is same as input signal frequency.

CIRCUIT DIAGRAMS:

LOW PASS FILTER



Design

Required cut off frequency f_H = 1 kHz

We have $f_H = \dfrac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$

Let $C_2 = C_3 = 0.0047\ \mu F$. Then $R_2 = R_3 = 33$ k.

For $R_2 = R_3$ and $C_2 = C_3$,

The pass-band gain $A_F = (1 + R_F/R_1)$ must be 1.586.

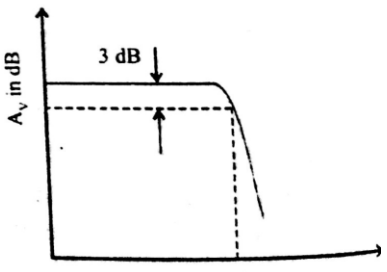
That is, $R_F = 0.586\ R_1$

Let $R_1 = 27$ k. Then $R_F = 15.82$ k. (Use 22 k pot)

Tabular column V_{in} = 1 volt

f (Hz)	V_O (V)	log (f)	A_V in dB

Graph



Exp No:4 **Date:**

SECOND ORDER LOW PASS AND HIGH PASS FILTERS

AIM:

To design and setup a second order low pass filter and high pass filters at high cut off frequency 1kHz.

APPRATUS REQUIRED:

The following devices and equipments are used to design and set up second order low pass and high pass filters.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	27KΩ,33KΩ (2),10KΩ, 15KΩ (2), 22KΩ(pot)	Each one
5	Capacitors	0.01uF, 0.0047uF	Each two
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

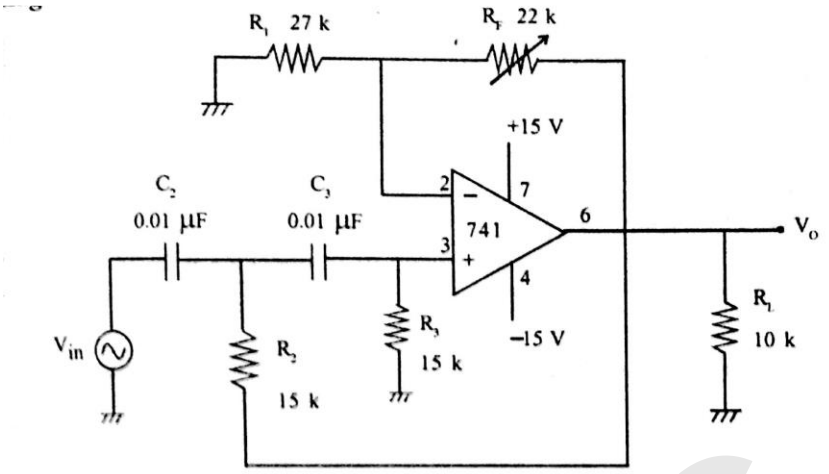
PRINCIPLE & PROCEDURE:

LPF: The roll-off second order filter is 40dB/decade. A first order low pass filter can be converted into a second order type simply by using an additional RC network. The gain of second order filter is set by Ri and Rf while the higher cut off frequency, f_H is determined by R_2, C_2, R_3 and C_3 as given by the expression, $f_H = 1/2\pi\sqrt{R_2R_3 C_2C_3}$
At low frequencies, both capacitors appear open and circuit becomes a voltage follower. As the frequency increases, the gain eventually starts to decrease.
HPF: A second order high pass filter can be constructed from a second order low pass filter by interchanging the frequency deciding resistors and capacitors. Consider the circuit diagram. At low frequencies, the capacitors appear open and voltage gain approaches to zero. At high frequencies, the capacitors appear short circuited and circuit becomes a non-inverting amplifier. The cut-off frequency of filter is given by the expression, $f_L = 1/2\pi\sqrt{R_2R_3 C_2C_3}$
If $R_2= R_3=R$ and $C_2= C_3=C$ $f_L= 1/2\pi\sqrt{RC}$

PROCEDURE:

1. Set up the circuits and feed a 2Vpp sine wave from the signal generator.
2. Vary the frequency in steps and note the output voltage.
3. Plot the frequency response.
4. Mark the lower cut-off frequency and calculate the roll-off in dB/decade.

HIGH PASS FILTER



Given cut off frequency f_L = 1 kHz We have, $f_L = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$

Take $C_2 = C_3 = C$ and $R_2 = R_3 = R$

Then $f_L = \frac{1}{2\pi RC}$

Assume, C = 0.01 µF. Then R = 15.9 k. Use 15 k std.

The pass-band gain $A_F = (1 + R_F/R_1)$ must be 1.586 for Butterworth filter.

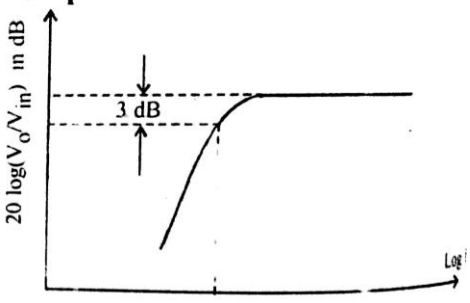
ie $R_2 = 0.586\ R_1$

Take $R_1 = 27$ K. Then $R_F = 15.82$ K use 22 k pot

Tabular column V_{in} = 1 volt

f in Hz	V_O volts	log (f)	A_V in dB

Graph



RESULT:

Designed and studied low pass and high pass filters.

INFERENCE:

Cut off frequency of LPF =……Hz
Cut off frequency of HPF =…….Hz

VIVA QUESTIONS:

1.What is a filter?

A filter is a frequency selective circuit that passes a specified band of frequencies and blocks a specified the frequencies outside the band.

2. State the advantage of active filters over passive?

a) Gain and frequency adjustment flexibility
b) No loading problems
c) Low cost
d) Absence of inductors makes the circuit work for high frequency applications.

3.Define order of a filter?

The number of RC networks employed in filter circuits represents the order of the circuit.

4.What are the types of active filters?

a) Low pass filter
b) High pass filter
c) Band pass filter
d) Band reject filter.

5.What is frequency response?

The variation of gain in decibels with respect to frequency is called frequency response.

6.What is the significance of 3 db line in frequency response?

Rms value of sine wave = 0.707
20 log(0.707) = -3db.
The 3 db line gives the cut off frequency.

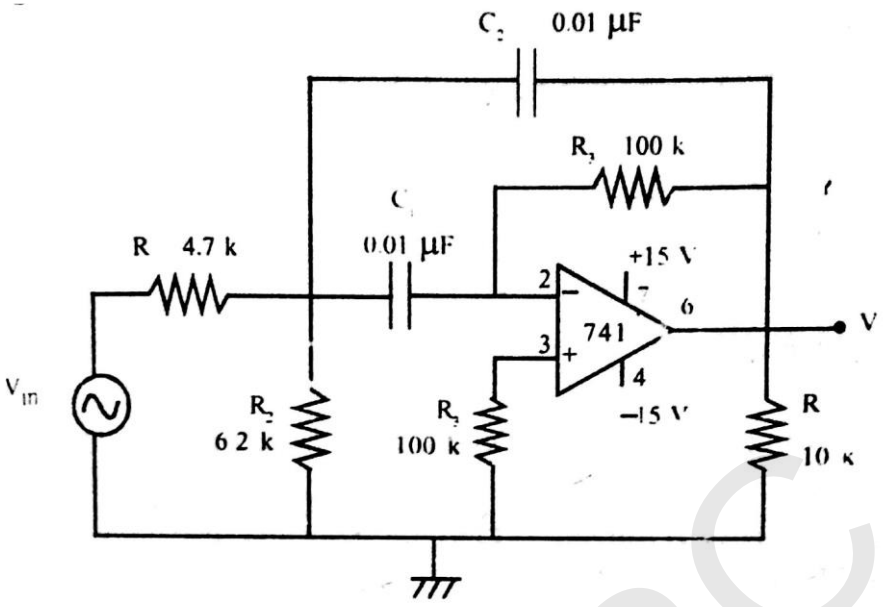
7.What are the applications of filters?

a) Communication circuits
b) Transmission

8. How do you classify active filters based on damping ratio?

a) Chebyshev
b) Butterworth

BAND PASS FILTER



Take $C_1 = C_2 = C = 0.01\ \mu F$

$$R = \frac{3}{2\pi(10^3)(0.01\times10^{-6})} = 4.77\ k\ (4.7\ k\ std)$$

$$R_2 = \frac{}{2\pi(10^3)(10^{-8})\ 18 - 10)} = 5.97\ k\ (5.6\ k\ std)$$

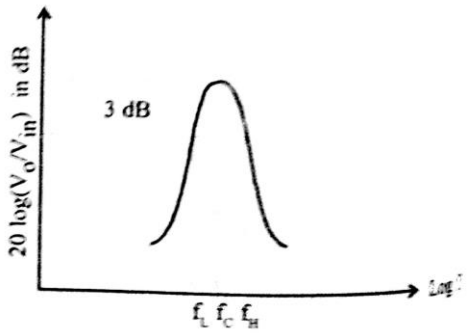
$$R_3 = \frac{3}{\pi(10^3)(10^{-8})} = 95.5\ k\ (100\ k\ std)$$

Use $R = 10\ k$

Tabular column $V_{in} = 1$ volt

f (Hz)	V_O (volts)	log f	A_v in dB

Graph



Exp No:5 **Date:**

ACTIVE BAND PASS AND NOTCH FILTERS

AIM:

i) To design and set up a band pass filter with fo= 1KHz, Q=3 and gain=10 and to draw its response characteristics.
ii) To design and set up a narrow band elimination filter (notch filter) and to draw its response characteristics.

APPARATUS REQUIRED:

The following devices and equipments are used to design and set up band pass and notch filters.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	27KΩ,33KΩ (2),10KΩ, 15KΩ (2), 22KΩ (pot)	Each one
5	Capacitors	0.01uF, 0.0047uF	Each two
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

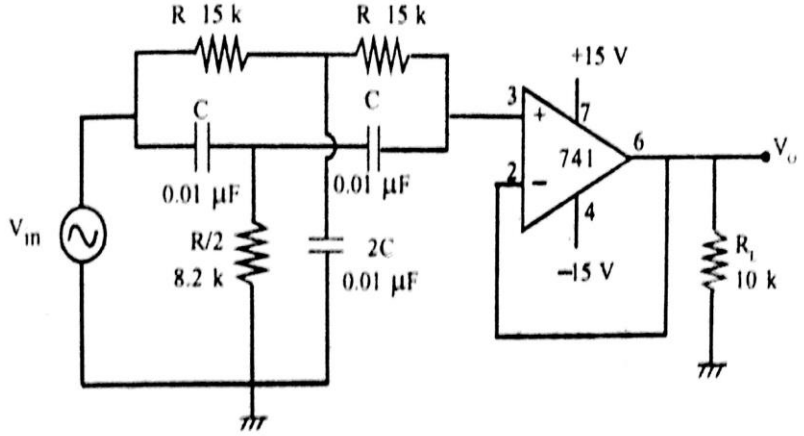
BPF: A band pass filter passes a particular band of frequencies with zero attenuation and attenuates all other frequencies. If an LPF with F_L is connected with HPF with F_H such that $f_H > f_L$, it forms BPF with bandwidth $f_H - f_L$.

Notch filter: Band elimination filter is also known as band rejection filter or band stop filter. Wideband rejection can be setup by connecting a low pass filter and a high pass filter in parallel. If an LPF with f_L is connected in parallel with HPF with f_H such that $f_H > f_L$, it forms BEF with bandwidth $f_H - f_L$. It provides maximum attenuation at f_0. This is achieved by a twin-T RC network. Passive twin T network has relatively low figure of merit Q. Q can be increased by associating with a voltage follower using op amp. Notch filter has wide applications in communication field. It is used to eliminate undesired frequencies. The very common application is to remove power supply that access at 50 Hz.

PROCEDURE:

1. Set the signal generator output as 1V sine wave.
2. Vary the frequency of sine wave and note down the output voltage.
3. Plot the frequency response on graph sheet.

BAND STOP FILTER



Design Required notch frequency $f_N = 1/2\pi RC = 1$ kHz

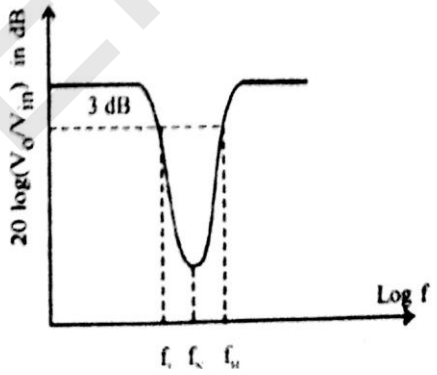
Take C = 0.01 μF. Then R = 15 k.

Take 2C = 0.01 μF and R/2 = 8.2 k.

Tabular column V_{in} = 1 volt

f in Hz	Vo volts	log (f)	A_V in dB

Graph



RESULT:

Designed and studied band pass and band stop filters.

INFERENCE:

Band pass filter:

Centre frequecncy f_o =…….
Bandwidth of the filter =……..
Q-factor of the filter =……...

Notch filter:

Centre frequency f_o =……..
Bandwidth of the filter =…….

VIVA QUESTIONS:

1. **What is the relation between f_C & f_H, f_L?**

$$f_C = \sqrt{f_H f_L}$$

2. **How do you increase the gain of the wideband pass filter?**

By increasing the gain of either LPF or HPF

3. **What is the difference between active and passive filters?**

Active filters use Op Amp as active element, and resistors and capacitors as the passive elements.

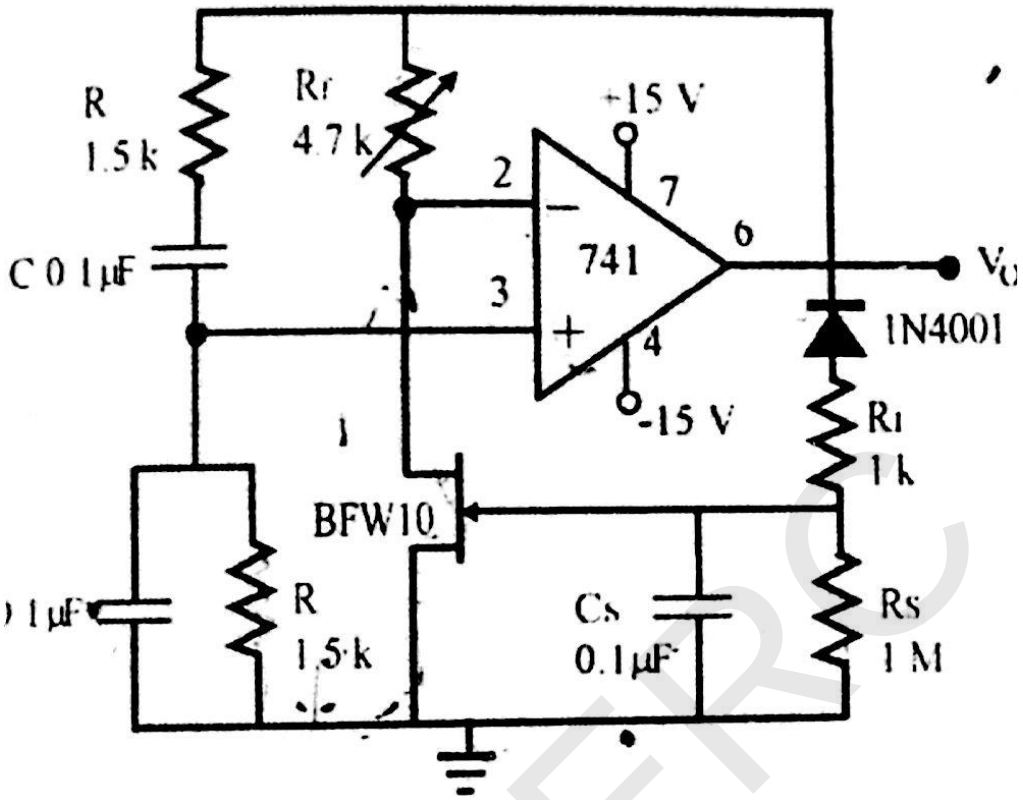
4. **What is the effect of order of the filter on frequency response characteristics?**

Each increase in order will produce -20 dB/decade additional increases in roll off rate.

5. **What modifications in circuit diagrams require to change the order of the filter?**

Order of the filter is changed by RC network.

CIRCUIT DIAGRAM:



DESIGN:

Required frequency $f_o = 1\ kHz$.

Given, $f_o = \frac{1}{2\pi RC}$

Let C be $0.1\ \mu F$. Then $R = 1.6\ k$

Use $1.5\ k$ std.

Gain $1 + \frac{R_f}{R_i} = 3$. Take $R_i = 1\ k$.

Then $R_f = 2.2\ k$. Use $4.7\ k$ potentiometer.

Select $R_S = 1\ M$ and $C_S = 0.1\ \mu F$.

Exp No:6 **Date:**

WIENBRIDGE OSCILLATOR WITH AMPLITUDE STAILIZATION

AIM:

To design set up a wien bridge oscillator incorporating amplitude stabilization.

APPARATUS REQUIRED:

The following components and equipments are used for wien bridge oscillator.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	1.5KΩ(2),1MΩ,4.7KΩ(po)	Each one
5	Capacitors	0.1uF	3
6	Diode	IN 4007	1
7	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

An FET circuit in association with the wien bridge oscillator, helps the stabilization of the amplitude of oscillation. The N-channel JFET acts as a voltage-controlled resistor and the diode circuit function as a negative peak detector. The dc voltage at the gate of FET becomes more negative when amplitude of oscillation increases. Then gate of FET gets reverse biased and effective resistance from drain to source increases. This causes to decrease the gain according to the relation $A=1+ (R_f /R_i)$ and amplitude is brought back to a stable level. When output peak starts to decrease, opposite patter occurs.

PROCEDURE:

1. Verify the conditions of op-amp and JFET.
2. Set up the circuit and observe the output waveform. Note down the frequency and amplitude of oscillation.

RESULT:

Designed and studied Wien bridge oscillator with amplitude stabilization and observed the waveform on CRO

INFERENCE:

Amplitude of the signal=……..V
Frequency of oscillation=……..Hz

VIVA QUESTIONS:

1.What is the oscillator?

The oscillator is a circuit that generates repetitive waveforms of fixed amplitudes and frequency without any external i/p signal.

2.What is the application of the oscillator?

A radio, T.V., Computers and communications.

3.What is the principle of the oscillator?

If the signal feedback is of proper magnitude and phase, the circuit produces alternating currents or voltage.

4.What are the two requirements for oscillation?

1. Magnitude of the loop gain must be at least 1
2.Total phase shift of the loop gain must be equal to 0 or 360 degree.

5.What is frequency stability?

The ability of the oscillator circuit to oscillate at one exact frequency is frequency stability.

6.What is the total phase for oscillation?

360 or 0 degree.

CIRCUIT DIAGRAMS:

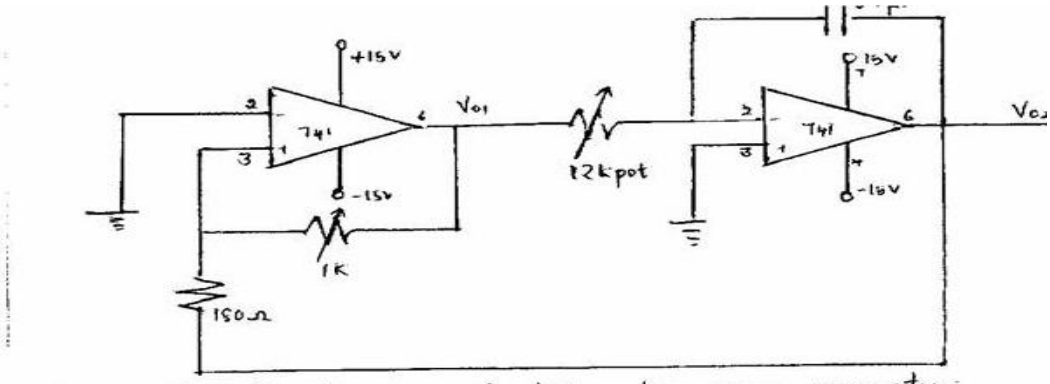


Fig (1): Circuit diagram of triangular wave generator

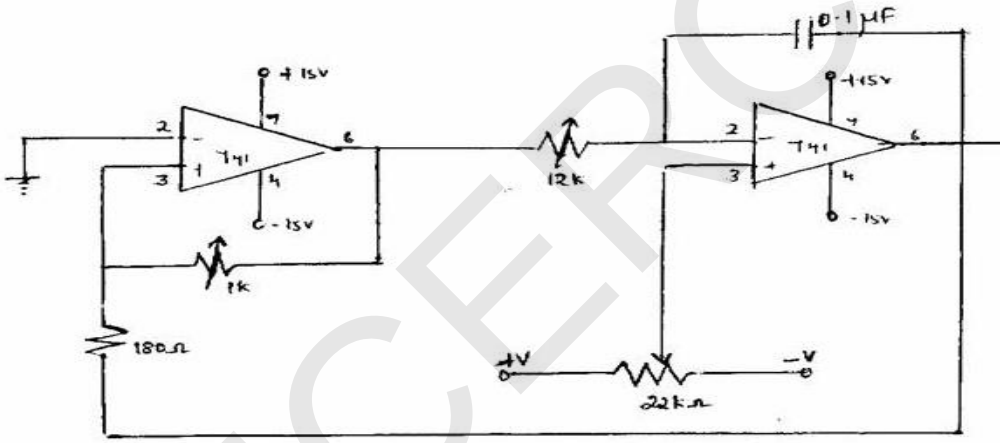


figure 2: Circuit diagram of sawtooth wave gener

DESIGN:

Triangular waveform generator:

frequency,f =R1/(4*R2*R3*C)
Peak-peak output of ramp Vpp = 2R2/R1
Let the required Vpp = 5V and Vsat = 13 V
Assume R1 = 1Kohm then R2 = 180 ohm
Take C = 0.1 microF, so R3 = 13 K
Sawtooth waveform generator:
frequency,f =R1/(4*R2*R3*C)
Peak-peak output of ramp Vpp = 2R2/R1
Let the required Vpp = 5V and Vsat = 13 V
Assume R1 = 1Kohm then R2 = 192 ohm Use 180-ohm standard
Take C = 0.1 microF, so R3 = 13 K Use 12K pot
Select R4 = 22 K

EXP NO: 7 **DATE:**

WAVEFORM GENERATOR USING OP AMP

AIM:

To set up and study a sawtooth and triangular wave form generator using Op-Amp for 1KHz frequency.

APPARATUS REQUIRED:

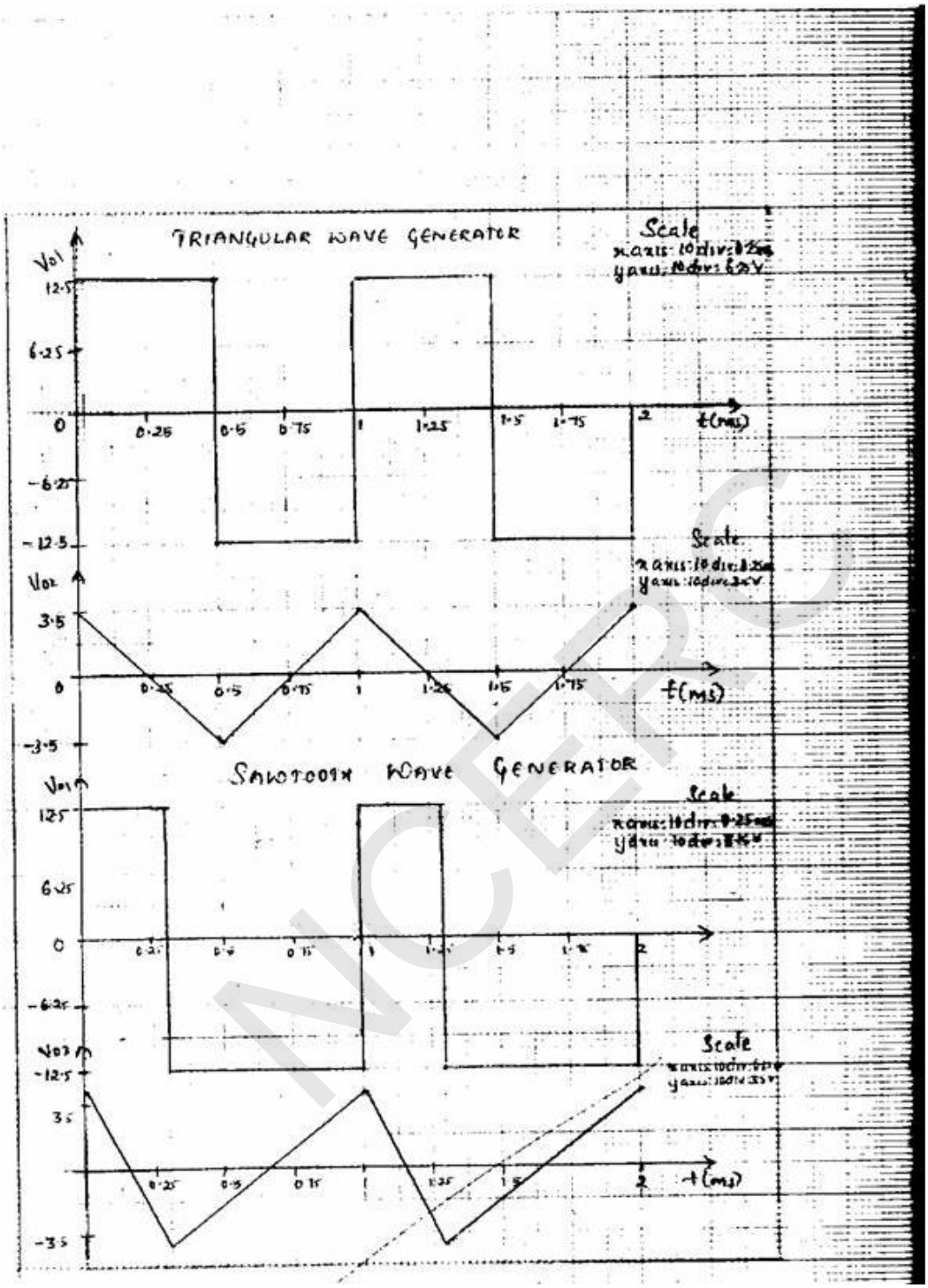
The following components and equipments are used for conducting the experiment

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
3	CRO		1
3	Resistors	180Ω,12KΩ(pot),1KΩ(pot), 22KΩ(pot)	Each one
4	Capacitors	0.1uF	1
5	Op-amp	741	2
6	Bread board	-	1
7	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

Triangular wave generator: This circuit uses two op-amps. One functions as a comparator and other as an integrator. Comparator compares the voltage at point P continuously with respect to the point voltage at the inverting input which is at zero volt. When voltage at P goes slightly above zero, the output of A will switch to negative saturation. Suppose the output of A is at positive saturation +Vsat, since this voltage is at the input of integrator, the output of A2 will be a negative going ramp. Thus one end of voltage divider R1 and R2 is at +Vsat and other end is at negative going ramp. At the time t=t1, when the negative going ramp attains the value of -Vramp, the effective voltage at P becomes slightly less than zero volt. This switches output of A1from +Vsat to –Vsat level. The output of A2 increases in the positive direction. At the instant t=t2 , voltage at P becomes just above zero volt thereby switching the output of A from –Vsat to + Vsat . The cycle repeats and generates a triangular waveform. Frequency of triangular waveform f = (R1/4R2R3C) .Peak to peak amplitude of ramp voltage is 2(R2/R1) Vsat.

Saw tooth waveform generator: In sawtooth waveform generator the rise time is much higher than its fall time or vice -versa. The triangular waveform generator can be converted into a Sawtooth waveform generator by including a variable dc voltage into non inverting terminal of the integrator.This can be done by using a port. When the wiper of the port is at the centre ,the output will be a triangular wave since the duty cycle is 50%.If the wiper moves towards negative ,the rise time of Sawtooth becomes larger than fall time. If the wiper moves towards positive ,the fall time becomes larger than rise time. The Sawtooth waveform generators have wide applications in time base generators and pulse width modulation circuits.


TRIANGULAR WAVE GENERATOR
Scale
Vo1
12.5
6.25
0
-6.25
-12.5
0.25
0.5
0.75
1
1.25
1.5
1.75
2
t(ms)
Scale
Vo2
3.5
0
-3.5
f(ms)
SAWTOOTH WAVE GENERATOR
Scale
Vo1
12.5
6.25
0
-6.25
Vo2
-12.5
3.5
-3.5
t(ms)

PROCEDURE:

1. Set up the waveform generator circuit.
2. Obtain the output and note down the amplitude and frequency.
3. Set up the circuit of sawtooth wave generator.
4. Observe the output of both op-amps and note down the rise time and fall time.
5. Obtain the output by moving the wiper of port in both directions and observe the changes taking place in waveforms.

RESULT:

Designed and Studied triangular and sawtooth wave generator circuits and the waveforms were observed on CRO

INFERENCE:

Amplitude and frequency of Square wave =……..…….V , ……..Hz
Amplitude and frequency of Triangular wave =…….V , ……..Hz
Amplitude and frequency of Sawtooth wave =…..…….V , ……..Hz

VIVA QUESTIONS:

1.What is a Schmitt trigger?

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform.

2.How is square wave generated?

Square wave is generated by using a comparator circuit.

3.How is triangular wave generated?

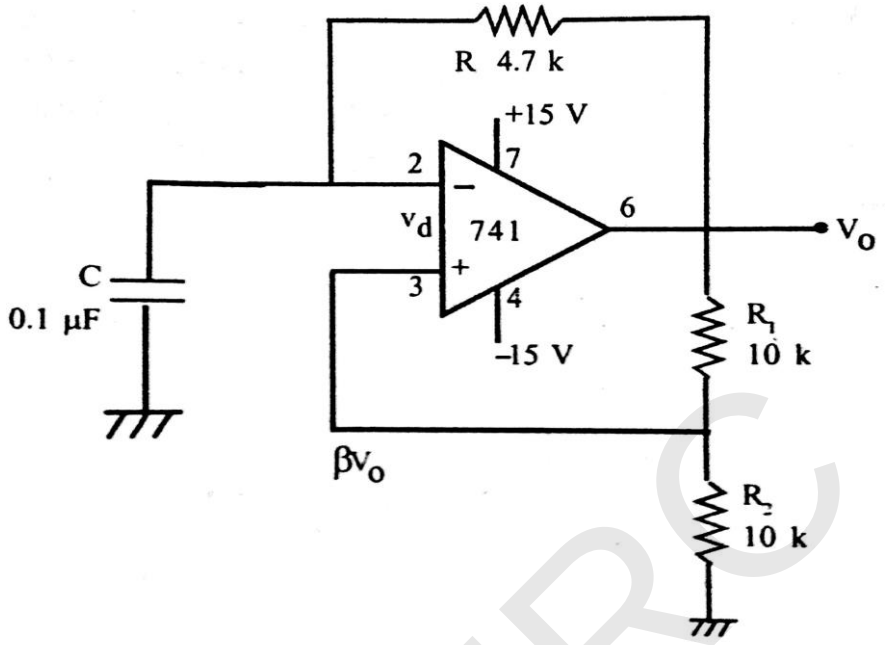
Square wave fed to a integrator circuit, we get triangular output.

4.How is sawtooth wave generated?

The triangular waveform generator can be converted into a sawtooth waveform generator by including a variable dc voltage into non inverting terminal of the integrator.This can be done by using a port

CIRCUIT DIAGRAMS:

ASTABLE MULTIVIBRATOR:



DESIGN:

Required period of oscillation T = 1 ms with duty cycle 50 %.

Time period $T = T_1 + T_2 = 2RC \ln(1 + \beta)/(1 - \beta)$

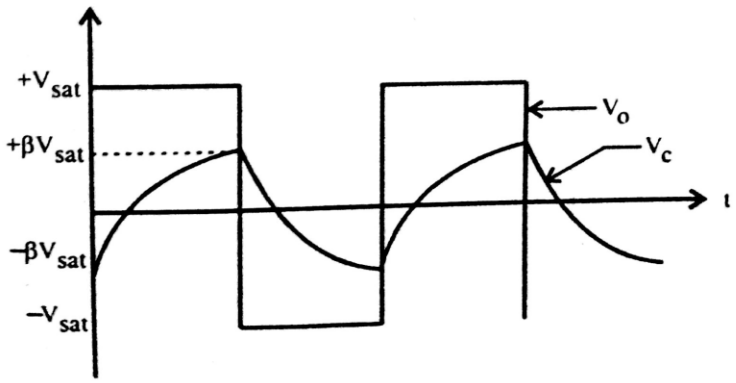
where β, the feedback factor $= R_2/(R_1 + R_2)$

Take $\beta = 0.5$ and $R_2 = 10$ k. Then $R_1 = 10$ k.

When $\beta = 0.5$, $T = 2.2\ RC$.

Let C be 0.1 μF. Then R = 4.7 k.

IS



Exp No:8 **Date:**

ASTABLE AND MONOSTABLE MULTIVIBRATORS USING OP-AMPS

AIM:

To design set up an astable and monostable multivibrator using op-amps for a frequency of 1kHz.

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment

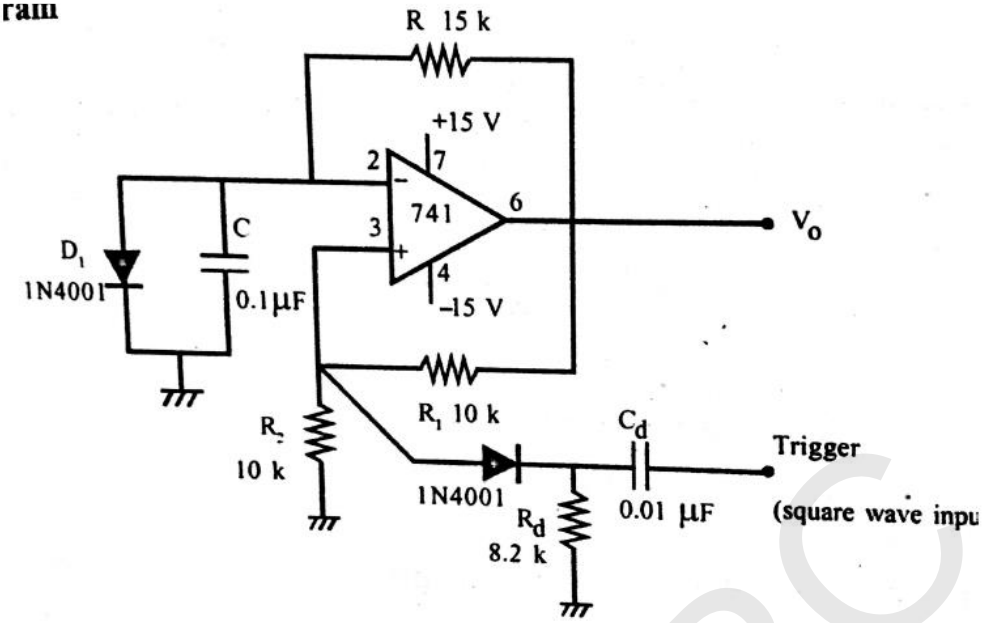
S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Functiongenerator	1MHz	1
3	CRO		1
4	Resistors	1.5KΩ(2),1MΩ,4.7KΩ(pot)	Each one
5	Capacitors	0.1uF	3
6	Diode	IN 4007	1
7	Op-amp	IC 741	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

ASTABLE MULTIVIBRATOR: Astable multivibrators are capable of producing square wave for given frequency, amplitude and duty cycle. The output of an op-amp is forced to swing repetitively between positive saturation $+V_{sat}$ and negative saturation $-V_{sat}$ resulting in asquare wave output. This circuit is also called free running multivibrator or square wave generator. The output of the op-amp will be in positive saturation if differential input voltage is negative and vice versa. The differential voltage $V_d = V_c - \beta V_{sat}$ where β is the feedback factor. βV_{sat} is the potential at non-inverting terminal of op-amp. Consider the instant at which $V_o=+V_{sat}$. Now the capacitor charges exponentially towards $+V_{sat}$ through R. Automatically V_d increases and crosses zero. This happens when V_c changes to $-V_{sat}$. Now capacitor starts to discharge to zero and recharge towards $-V_{sat}$. Now V_d decreases and crosses zero. This happens when $V_c=- \beta V_{sat}$. The moment V_d becomes negative again, output changes to $+V_{sat}$. This completes one cycle. The time period T of the square wave is $T= 2RC\ln(1+\beta)/(1-\beta)$. If β is made ½, T= 2.2RC. Astable multivibrator is particularly useful for the generation of frequency in the audio frequency range. Higher frequencies are limited by the delay time and slew rate of the op-amp.

MONOSTABLE MULTIVIBRATOR:

rain



Design We have, $T = RC \ln[1/(1-\beta)]$. Let $\beta = 0.5$. Then $T = 0.69RC$

Take T = 1 ms and C = 0.1 μF. Then R = 14.5 k. Use 15 k std.

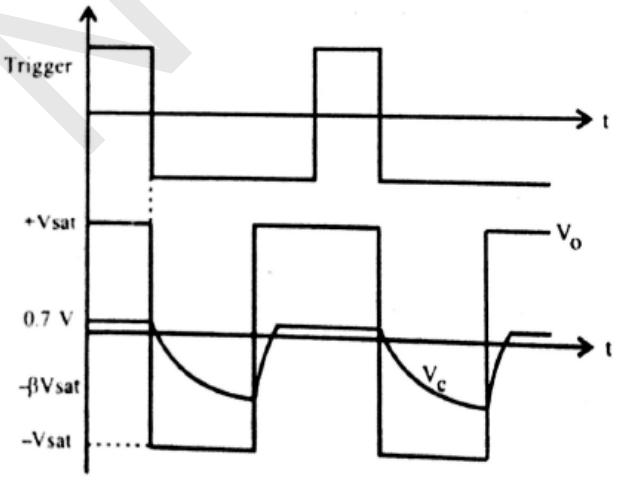
Since $\beta = R_2/(R_1 + R_2)$, $R_1 = R_2 = 10$ k.

Design of differentiating circuit: $R_dC_d < 0.016T_t$.

Take trigger time period T_t = 5 ms and C_d = 0.01 μF.

Then R_d = 8.2 k.

Waveforms



MONOSTABLE MULTIVIBRATOR: A Monostable Multivibrator, often called a one-shot Multivibrator. It has a stable state and and a quasi-stable state. The circuit remains in stable state until triggering signal causes a transition to quasi stable state. After a time interval, it returns to the stable state. So, a single pulse of predetermined duration can be generated using this circuit. Consider the instant at which the output $V_o=+V_{sat}$. Now the diode D1 clamps the capacitor voltage V_c at 0.7V. feedback voltage available at non inverting terminal is $+\beta V_{sat}$. When the negative going trigger is applied such that potential at non inverting terminal becomes less than 0.7 V, the output switches to $-V_{sat}$. Now the capacitor charges through R towards –Vsat, because the diode becomes reverse biased. When the capacitor voltage become more negative than –Vsat, the comparator switches back to $+V_{sat}$, and the capacitor C starts charging to $+V_{sat}$ through R until V_c reaches 0.7.

PROCEDURE:

1. Verify the conditions of op-amp.
2. Set up the circuit astable multivibrator and observe the output waveform. Note down their frequencies and amplitudes.
3. Set up the circuit monostable multivibrator and feed 6Vpp,300Hz pulse at the trigger input and observe the output waveform. Note down their frequencies and amplitudes.

RESULT:

Designed and studied astable and monostable multivibrators using op-amps and the waveforms were observed on CRO

INFERENCE:

Amplitude and Frequency of the astable square ouput=……V , ……..Hz
Amplitude and Frequency of the monostable square ouput =……V ,……Hz

VIVA QUESTIONS:

1. **Is the triggering given is edge type or level type? If it is edge type, trailing or raising edge?**

   Edge type and it is trailing edge

2. **What is the effect of amplitude and frequency of trigger on the output?**

   Output varies proportionally.

3. **How to achieve variation of output pulse width over fine and course ranges?**

One can achieve variation of output pulse width over fine and course ranges by varying capacitor and resistor values respectively.

4. **What is the effect of Vcc on output?**

   The amplitude of the output signal is directly proportional to Vcc.

5. **What are the ideal charging and discharging time constants (in terms of R and C) of capacitor voltage?**

   Charging time constant T=1.1RC Sec
   Discharging time constant=0 Sec

6. **What is the other name of monostable Multivibrator? Why?**

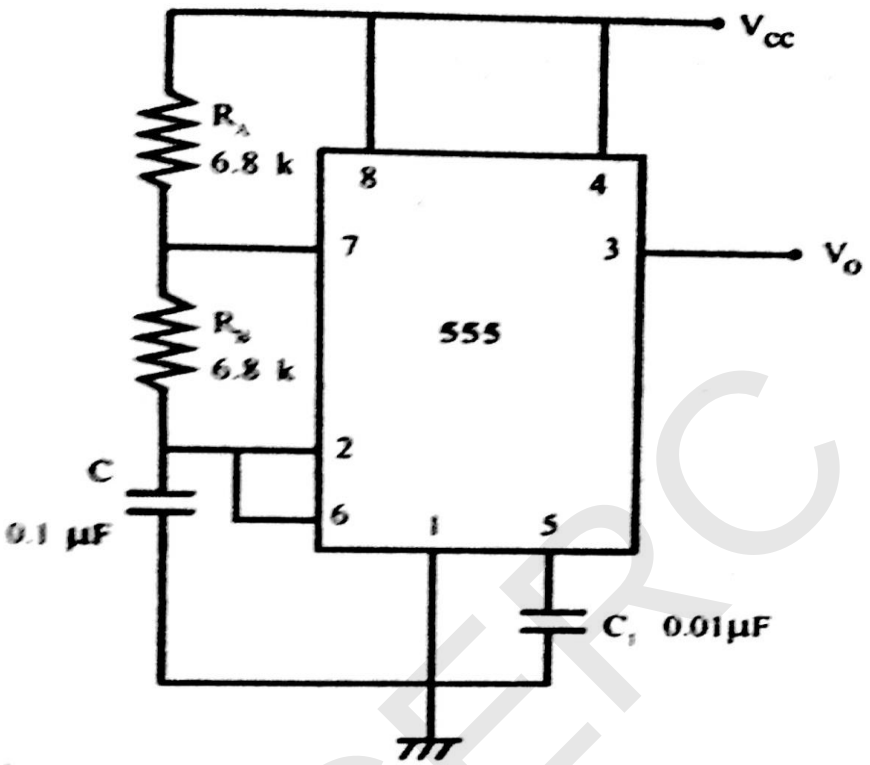
   i) Gating circuit .It generates rectangular waveform at a definite time and thus could be used in gate parts of the system.
   ii) One shot circuit. The circuit will remain in the stable state until a trigger pulse is received. The circuit then changes states for a specified period, but then it returns to the original state.

7. **What are the applications of monostable Multivibrator?**

   Missing Pulse Detector, Frequency Divider, PWM, Linear Ramp Generator

CIRCUIT DIAGRAMS:

ASTABLE MULTIVIBRATOR:



DESIGN:

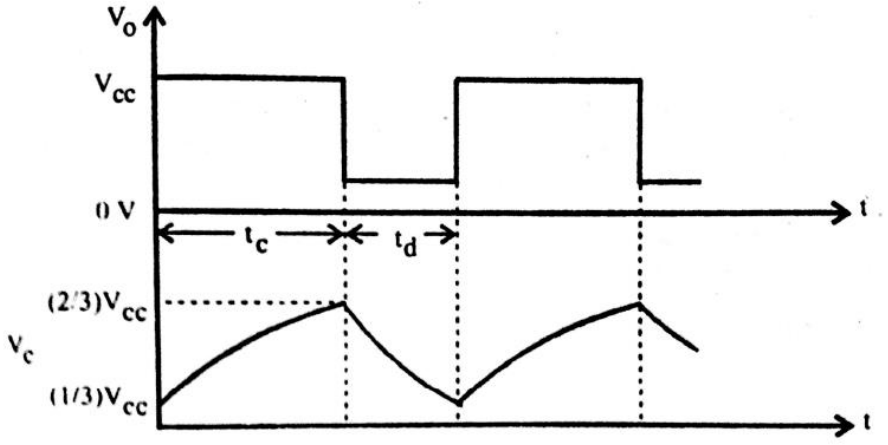
Take V_{cc} = 10 V and t_c = 1 ms and t_d = 0.5 ms

We have, $t_c = 0.69(R_A + R_B)C$ and $t_d = 0.69R_BC$

The R_A and R_B should be in the range of 1 k to 10 k to limit the collector current of the internal transistor. Take $R_A = R_B$ = 6.8 k.

Let C = 0.1 μF. Choose C_1 = 0.01 μF

Waveform:



Exp No: 9 **Date:**

ASTABLE AND MONOSTABLE MULTIVIBRATORS USNIG IC 555

AIM:

To design set up a astable and monostable multivibrators usnig IC 555 for a frequency of 1kHz.

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	10 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	6.8KΩ(2),10KΩ,5.6KΩ	Each one
5	Capacitors	0.1uF,0.01uF(2)	Each one
6	diode	IN 4007	1
7	Timer IC	555	1
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

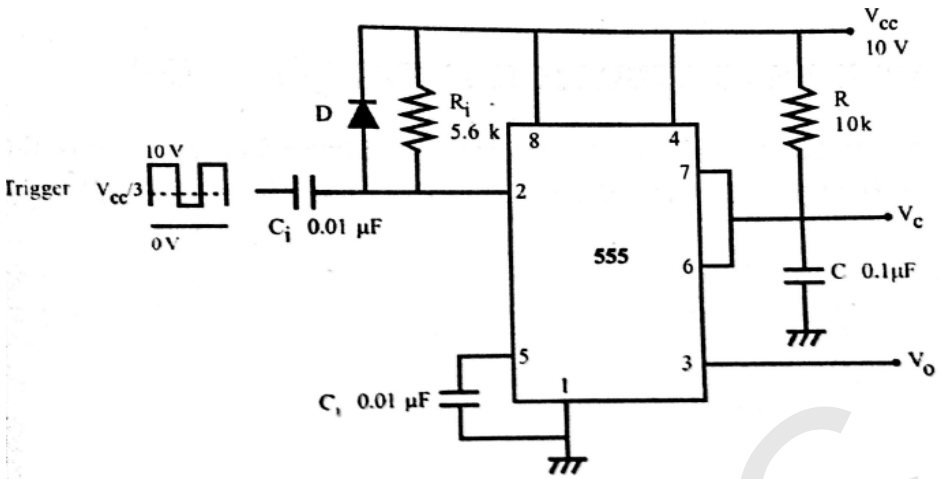
ASTABLE MULTIVIBRATOR: When the power supply V_{CC} is connected, the external timing capacitor 'C" charges towards V_{CC} with a time constant (R_A+R_B) C. During this time, pin 3 is high ($\approx V_{CC}$) as Reset R=0, Set S=1 and this combination makes $\overline{Q}$=0 which has unclamped the timing capacitor 'C'.

When the capacitor voltage equals 2/3 V_{CC}, the upper comparator triggers the control flip flop on that $\overline{Q}$=1. It makes Q1 ON and capacitor 'C' starts discharging towards ground through R_B and transistor Q1 with a time constant R_BC. Current also flows into Q1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q1. The minimum value of R_A is approximately equal to $V_{CC}/0.2$ where 0.2A is the maximum current through the ON transistor Q1.

During the discharge of the timing capacitor C, as it reaches $V_{CC}/3$, the lower comparator is triggered and at this stage S=1, R=0 which turns $\overline{Q}$=0. Now $\overline{Q}$=0 unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between 2/3 V_{CC} and 1/3 V_{CC} respectively. The length of time that the output remains HIGH is the time for the capacitor to charge from 1/3 V_{CC} to 2/3 V_{CC}.

The charging period of capacitor = 0.69 $(R_A + R_B)$ C.
The discharging period of capacitor = 0.69 R_B C.

MONOSTABLE MULTIVIBRATOR:



Design Take V_{cc} = 10 V and T = 1 ms

We have, T = 1.1 RC.

Take R = 10 k to limit current through the internal transistor to 1 mA.

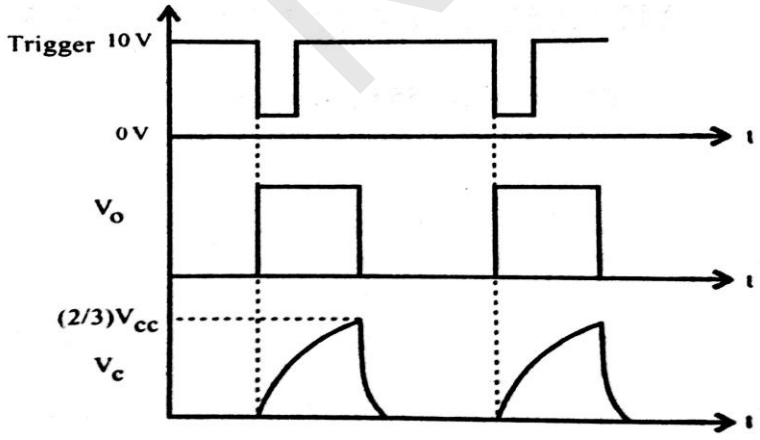
Then C = 0.1 μF.

Design of triggering circuit We have, $R_iC_i \leq 0.0016T_t$ where T_t is the time period of the trigger.

Take T_t = 3 ms.

Take R_i = 5.6 k to avoid loading. Then C_i = 0.01 μF. Choose C_1 = 0.01 μF.

Waveform:



MONOSTABLE MULTIVIBRATOR: A Monostable Multivibrator, often called a one-shot Multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer. In a stable or standby mode $\overline{Q}$ is high and in turn, Q1 is turned ON and output is low. When the negative going trigger passes through $V_{CC}/3$, the FF is set i.e., $\overline{Q}=0$. This makes transistor Q1 off. The capacitor starts charging towards V_{CC}, which was earlier clamped to zero. After a time period, the capacitor voltage becomes greater than 2/3 V_{CC} and upper comparator resets the FF, i.e., R=1, S=0. This makes $\overline{Q}=1$. In turn the transistor Q1 turns ON and thereby discharging the capacitor C rapidly to ground potential. Mononostable circuit has only one stable state (output low), hence the name monostable. Normally the output of the Monostable Multivibrator is low.

PROCEDURE:

1. Set up the astable multivibrator circuit after verifying the condition of the IC
2.Observe the output waveform at pin no.3 and 6 of the IC.
3. Set up the monostable multivibrator circuit.
4. Use positive pulses of amplitude Vcc and frequency 300 Hz as the trigger.
5. Observe the output waveform at pin no.3 and 6 of the IC

RESULT:

Designed and studied astable and monostable multivibrators using timer IC and the waveforms were observed on CRO

INFERENCE:

Amplitude and Frequency of the astable square ouput=……V , ……..Hz
Amplitude and Frequency of the monostable square ouput =……V ,……Hz

VIVA QUESTIONS:

1. **How do you vary the duty cycle?**

   By varying R_A or R_B.

2. **What are the applications of 555 in astable mode?**

   FSK Generator, Pulse Position Modulator, Square wave generator

3. **What is the function of diode in the circuit?**

   To get symmetrical square wave.

4. **On what parameters T_c and T_d designed?**

   R_A ,R_B and C

5. **What are charging and discharging times?**

   The time during which the capacitor charges from (1/3) Vcc to (2/3) Vcc is equal to the time the output is high is known as charging time and is given by $T_c=0.69(R_A+R_B)$ C

   The time during which the capacitor discharges from (2/3) Vcc to (1/3) Vcc is equal to the time the output is low is known as discharging time and is given by $T_d=0.69(R_B)$ C.

6. **What is quasi stable state?**

   Change from one state to another without any external trigger is termed as quasi stable state.

7. **What are the various modes of operation of multivibrator? Explain**

   Astable mode – 2 quasi stable state
   Monostable – 1 quasi and on stable state.
   Bistable – 2 stable states.

8. **What is one-shot multivibrator?**

   The monostable is also called as one-shot multivibrator as it produces a single pulse of specified duration in response to each external trigger signal. Only one stable state exists. When an external trigger signal is applied the output changes its state.

9. **What is the advantage of 555 IC over op amp?**

   555 IC generates accurate time delay compared to op amp.

10. List the basic blocks of IC 555 timer?

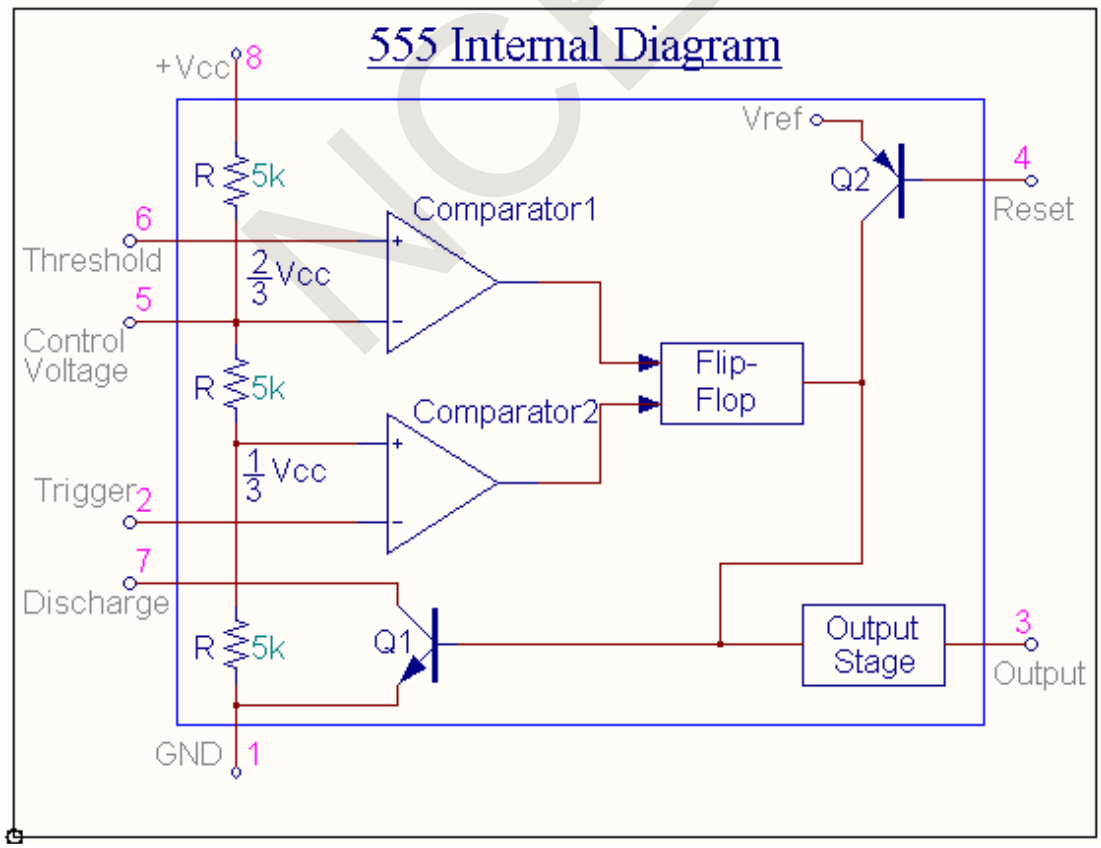
- A relaxation oscillator.
- R-S flip-flop
- Two comparators
- Discharge transistors.

11. Give the applications of 555-timer Astable multivibrator.

a) Square wave generator
b) Voltage Controlled Oscillator (VCO)
c) FSK Generator
d) Schmitt trigger.

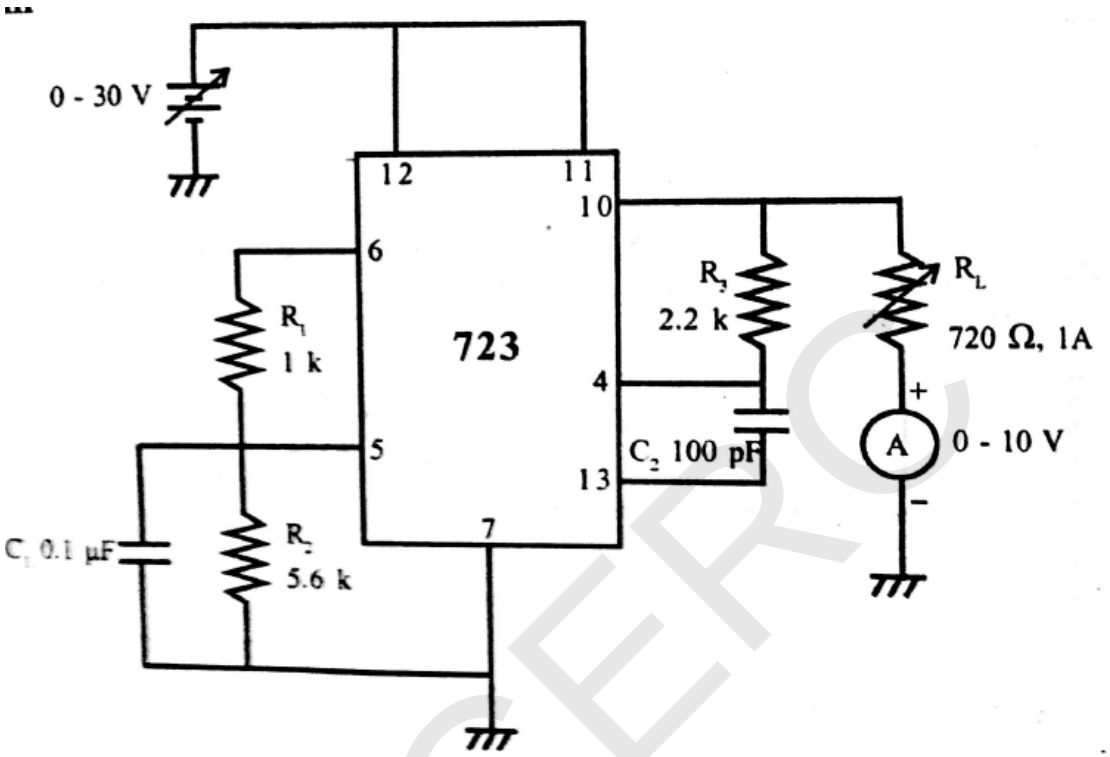
12. List the applications of monostable mode of 555 timer.

a) Missing Pulse detector
b) Linear ramp generator
c) Frequency divider



CIRCUIT DIAGRAMS:

LOW VOLTAGE REGULATOR:



DESIGN:

Use 14 pin DIP 723. $V_O = 7.15\ (R_2/(R_1 + R_2) = 6$ V

Let the divider current I_D through the resistor-divider R_1 and R_2 be 1 mA. Since error amplifier draws very little current, we will neglect its input bias current.

Hence, $R_1 = \dfrac{V_{ref} - V_O}{I_D} = \dfrac{7.15 - 6}{1\text{ mA}} = 1.1$ k. Use 1 k std.

$R_2 = \dfrac{V_O}{I_D} = \dfrac{6}{1\text{ mA}} = 6$ k. Use 5.6 k std.

For stability $R_3 = \dfrac{R_1 R_2}{R_1 + R_2}$. As per data sheet $1K < R_3 < 3.52\ K$

Take $R_3 = 2.2K$. choose $C_1 = 0.1$uf and $C_2 = 100$ pf

Exp No:10 **Date:**

DC POWER SUPPLY USING IC 723

AIM:

i) To design and set up a low voltage regulator for an output voltage of 6V
ii) To design and set up a high voltage regulator for an output voltage of 12V

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	0-30V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	10KΩ (2),15KΩ,5.6KΩ.2.2KΩ, 1KΩ	Each one
5	Capacitors	0.1uF.100pF	3
6	Regulator IC	IC 723	1
7	Rheostat	720Ω,1 A	1
8	Bread board	-	1
9	Connecting wires	-	As required

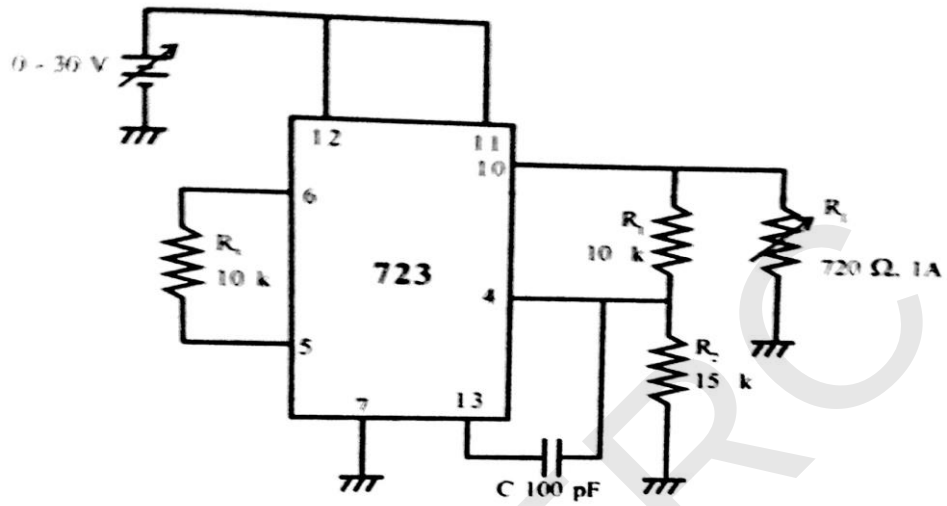
PRINCIPLE & PROCEDURE:

LOW VOLTAGE REGULATOR : In order to understand the working, consider the functional block diagram of the low voltage regulator V_{ref} point is connected through a resistance to the non-inverting terminal and the output is feed back to the inverting terminal of the error amplifier. If the output voltage becomes low, the voltage at the inverting terminal of the error amplifier also goes down. This makes the output of the error amplifier become more positive, there by driving the Q1 transistor more into conduction. This reduce the voltage across Q1 and drives more current into the load causing voltage across load to increase. Thus the initial decrease in the load voltage is compensated. Similarly, any increase in the load voltage gets regulated. A close examination of the circuit will show that the error amplifier functions as a voltage follower. The voltage at the non-inverting terminal is $7.15(R_2/R_1+R_2)$.

HIGH VOLTAGE REGULATOR : If it is desired to produce regulated output voltage greater than 7V, a small change should be made in the circuit for low voltage regulator. The non-inverting terminal is connected directly to V_{ref} through R3. So the voltage at the non-inverting terminal is V_{ref}. The error amplifier operates as a non-inverting amplifier with a voltage gain of $Av=1+R_1/R_2$. Notice that Av is always greater than 1. So the output voltage of the circuit is $Vo=7.15(1+ R_1/R_2)$.

CIRCUIT DIAGRAMS:

HIGH VOLTAGE REGULATOR:



DESIGN:

Required output voltage $V_O = 12$ V.

V_O is given by the expression, $V_O = 7.15(1 + R_1/R_2)$

Take $R_1 = 10$ k. Then $R_2 = 17.7$ k. Use 15 k std.

Take $R_L = 720\ \Omega$ rheostat and C = 100 pF

Tabular column

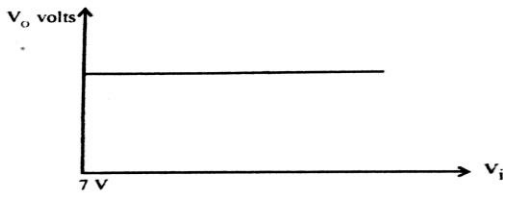
Line regulation

V_i (volts)	V_O (volts)

Load regulation

V_O volts	I_O mA

Graph



PROCEDURE:

Low voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from 6V to 15V and observe the output voltage. Note down it in tabular column.
3. Vary the rheostat and note the change in output current.
4. Draw the regulation characteristics with input on X-axis and output on Y-axis.
5. Calculate the % line regulation using the expression:
   S_V = change in output voltage / change in input voltage
6. Calculate the % load regulation using the expression:
   $S_L = (V_{NL} – V_{FL})/ V_{NL}$

High voltage regulator:

1. Set up the circuit. Switch on the power supply and input voltage sources.
2. Vary the input voltage from 6V to 30V and observe the output voltage. Note down it in tabular column.
3. Vary the rheostat and note the change in output current.
4. Draw the regulation characteristics with input on X-axis and output on Y-axis.
5. Calculate the % line regulation using the expression:
   S_V = change in output voltage / change in input voltage
6. Calculate the % load regulation using the expression:
   $S_L = (V_{NL} – V_{FL})/ V_{NL}$

RESULT:

Designed and studied low voltage regulator and high voltage regulator circuits.

INFERENCE:

Low voltage regulator:
% Line regulation=…….
% Load regulation=…….

Low voltage regulator:
% Line regulation=…….
% Load regulation=…….

VIVA QUESTIONS:

1. **What is the main function of voltage regulator?**

   The main function of a voltage regulator is to provide a stable DC voltage for processing other electronic circuits.

2. **What are the different types of voltage regulators?**

   a) Fixed output voltage regulator (positive or negative)
   b) Adjustable output voltage regulators (positive or negative)
   c) Switching regulators.
   d) Special regulators.

3. **What are switching regulators?**

   Regulators which operate the transistor as a high frequency ON/OFF switch, so that the power transistor does not conduct current continuously is called switching regulator.

4. **What are the four main parts of voltage regulators?**

   a) Reference voltage circuit b) Error amplifier
   c) Series pole transistor d) Feedback Network.

5. **What are the main advantages of voltage regulators?**

   a) Short circuit Protection. b) Output Voltage can be varied.

6. **Define line regulation or source regulation**.

   Line regulation is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as % of the input voltage.

7. **Define Load regulation.**

   Load regulation is defined as the change in regulated output voltage for a change in load current. It is usually expressed in millivolts or as a percentage of the output voltage.

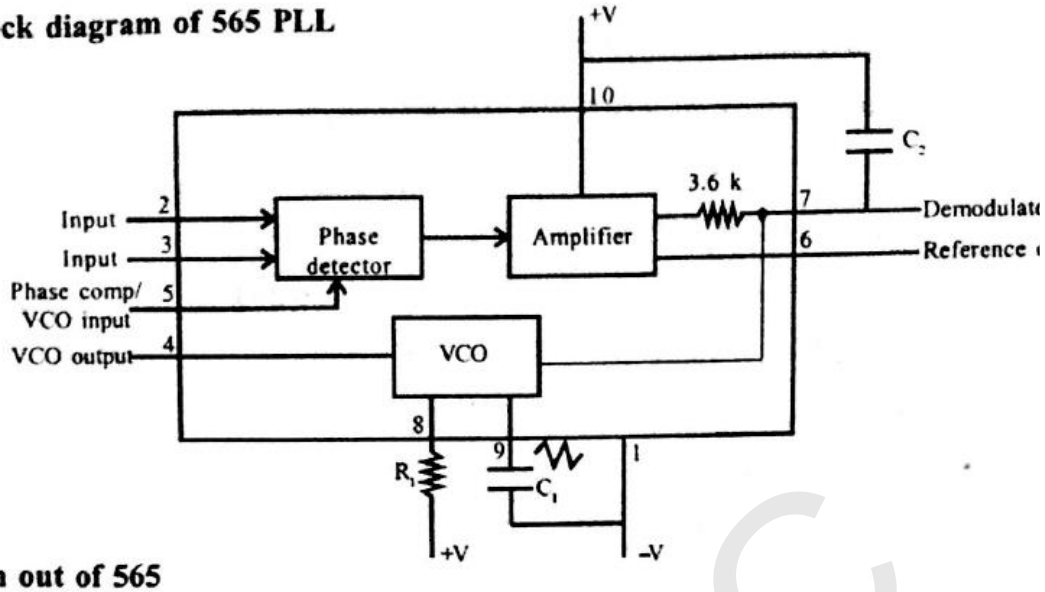
8. **What are the limitations of 723 regulators?**

   a) No built-in thermal protection. b) It has no short circuit current limits.

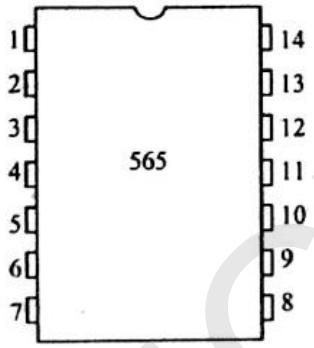
9. **What is current limiting ability?**

   Current limiting ability refers to the ability of the regulator to prevent the load current from increasing above a preset value.

Block diagram of 565 PLL

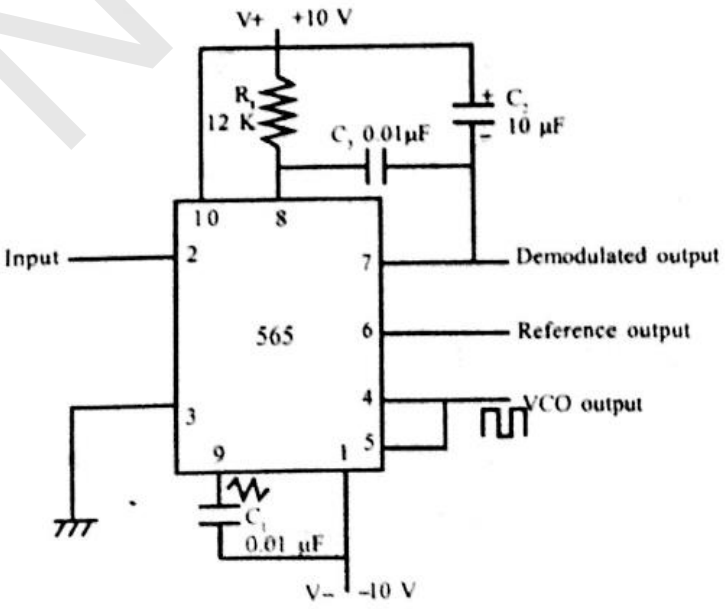


Pin out of 565



1. V-
2. Input
3. GND
4. VCO output
5. Phase comparator/VCO input
6. Reference output
7. Demodulated output
8. External R for VCO
9. External C for VCO
10. V+
11 to 14: NC

Circuit diagram



Exp No:11 **Date:**

STUDY OF PLL IC: FREE RUNNING FREQUENCY LOCK RANGE CAPTURE RANGE

AIM:

To design set up a PLL circuit and study its functional characteristics.

APPARATUS REQUIRED:

The following components and equipments are used for the design of 565 PLL.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±10 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	12KΩ (2)	Each one
5	Capacitors	0.01uF (2),10uF	Each one
6	PLL IC	565	1
7	Bread board	-	1
8	Connecting wires		As required

PRINCIPLE & PROCEDURE:

PLL is a control system that generates an output signal whose phase is related to the phase of input reference signal. It mainly consists of a phase detector, an LPF and a VCO. Phase comparator or phase detector compare the frequency of input signal f_s with frequency of VCO output f_o and it generates a signal which is function of difference between the phase of input signal and phase of feedback signal which is basically a d.c voltage mixed with high frequency noise. LPF remove high frequency noise voltage. Output is error voltage. If control voltage of VCO is 0, then frequency is center frequency (f_o) and mode is free running mode. Application of control voltage shifts the output frequency of VCO from f_o to f. On application of error voltage, difference between f_s & f tends to decrease and VCO is said to be locked. While in locked condition, the PLL tracks the changes of frequency of input signal.

Center frequency (free running frequency) $f_o = 1.2/4R_1C_1$ Hz

Lock range $f_L = \pm 8\, f_o/V$ Hz

$V = (+V) - (-V)$

Capture range $f_c = \pm \left[\dfrac{f_L}{2\Pi(3.6)x10^3 xC2} \right]^{1/2}$

PROCEDURE:

1. Verify the condition of components.
2. Set up the circuit and observe the output waveform and note down the VCO frequency.

Design Take V+ = +10 V and V– = – 10 V

Let the free running frequency f_0 be 2.5 kHz $= \frac{1.2}{4R_1C_1}$

Take $C_1 = 0.01\ \mu F$ Then $R_1 = 12$ k

The value of R_1 satisfies the required condition 2 k < R_2

Take $C_3 = 0.01\ \mu F$ $C_2 = 10\ \mu F$

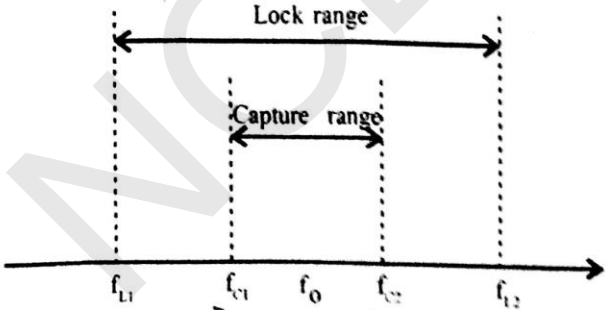
Theoretical values of f_L and f_C

$$f_L = \pm \frac{8x2.5x10^3}{10-(-10)} = \pm 1 \text{ kHz}$$

$$f_C = \frac{\sqrt{10^3}}{\sqrt{2\pi x3.6x10^{3)} x10x10^{-6}}} = 66.5 \text{ Hz}$$

Take $C_3 = 0.01\ \mu F$ $C_2 = 10\ \mu F$

Graph



3. Feed a square wave to the pin no.2 of 565 PLL IC and vary its frequency from 100Hz to 1MHz and note down f_{C1} and $f_{L2.}$ Then decrease the frequency from 1MHz to 100Hz note down f_{C2} and f_{L1}
4.Calculate capture range and lock range.

RESULT:

Studied the functional characteristics of 565 PLL.

INFERENCE:

Free running frequency =……..Hz
Lock range =……Hz
Capture range =…….……Hz

VIVA QUESTIONS:

1. **What is phase locked loop?**

   It is a circuit which provides frequency selective tuning and filtering without coils or inductors.

2. **List the components of the block diagram of PLL.**

   a) Phase detector b) Low pass filter c) Error amplifier d) Voltage controlled Oscillator.

3. **What is voltage-controlled oscillator?**

   Oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

4. **Define pull in time.**

   The total time taken by the PLL to establish lock.

5. **Define Lock-in range.**

   The range of frequencies over which PLL can maintain lock with the incoming signal.

6. **Define capture range**.

   The range of frequencies over which PLL can acquire lock with the input signal.

7. **What are the applications of PLL?**

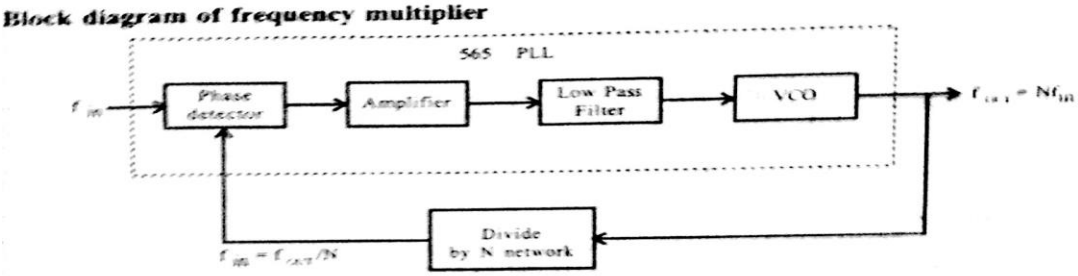
   a) FM Modulation
   b) Signal generation
   c) Frequency shift keying
   d) Frequency multipliers

8. **What are the 3 stages of PLL characteristic?**

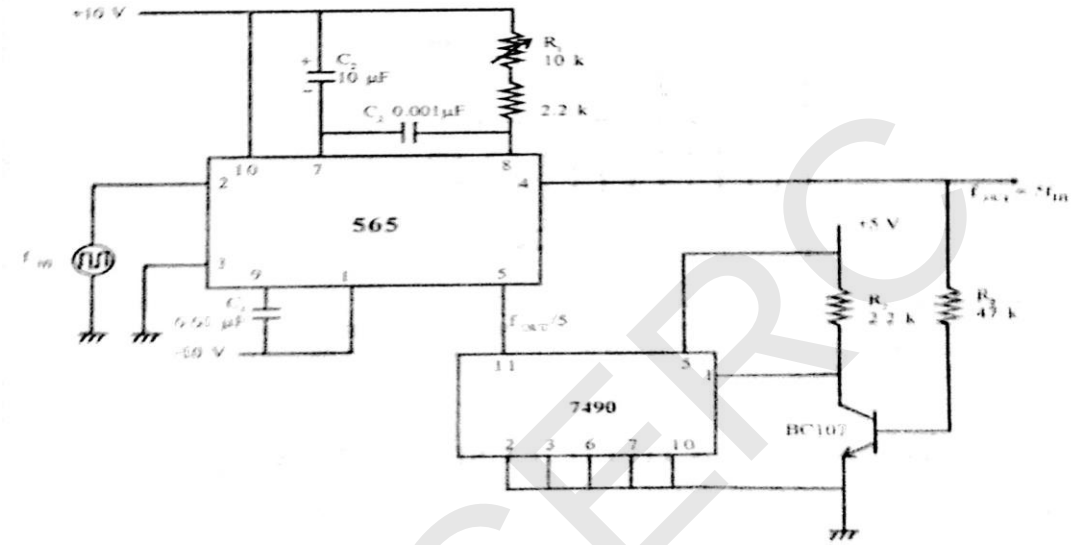
   a) Free running
   b) Capture
   c) Locking.

CIRCUIT DIAGRAM:

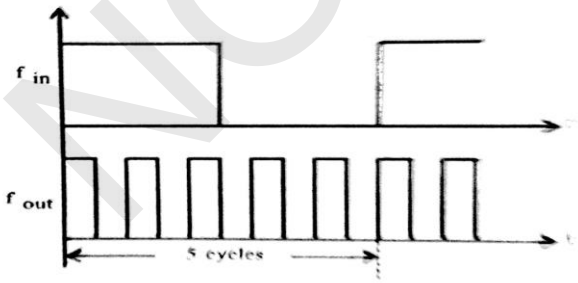
Block diagram of frequency multiplier



Circuit diagram



Waveforms



Exp No:12 **Date:**

APPLICATION USING PLL-FREQUENCY MULTIPLICATION

AIM:

To design set up a frequency multiplier circuit using 565 PLL.

APPARATUS REQUIRED:

The following components and equipments are used for the design of frequency multiplier.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	±10 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	10KΩ(pot),2,2KΩ(2), 47KΩ	Each one
5	Capacitors	0.01uF(2),10uF	Each one
6	PLL IC	565	1
7	Decade counter IC	IC 7490	1
8	Transistor	BC 107	1
9	Bread board	-	1
10	Connecting wires		As required

PRINCIPLE & PROCEDURE:

In a frequency multiplier using PLL 565, a divided by N network is inserted between the VCO output and the phase comparator input. Since the output of the comparator is locked to the input frequency f_{in} the VCO is running at a multiple of the input frequency. Therefore, in the locked state the VCO output frequency is given by,
$f_0 = Nf_{in}$

PROCEDURE:

1. Set up the counter and verify it's working.
2. Complete the circuit and feed 5 V, 2KHz pulses to pin no.2 of 565 IC.
3. Observe the multiplied frequency at pin no.4

RESULT:

Studied the frequency multiplier circuit using 565 PLL.

INFERENCE:

Frequency of the multiplied signal =……Hz

VIVA QUESTIONS:

1. Mention the applications of PLL

Frequency multiplier
Frequency synthesizer
Frequency translation
Clock and data recovery

2. What is a voltage controlled oscillator?

Voltage controlled oscillator is a free running multivibrator operating at a set frequency called the free running frequency. This frequency can be shifted to either side by applying a dc control voltage and the frequency deviation is proportional to the dc control voltage.

3. What are the applications of VCO?

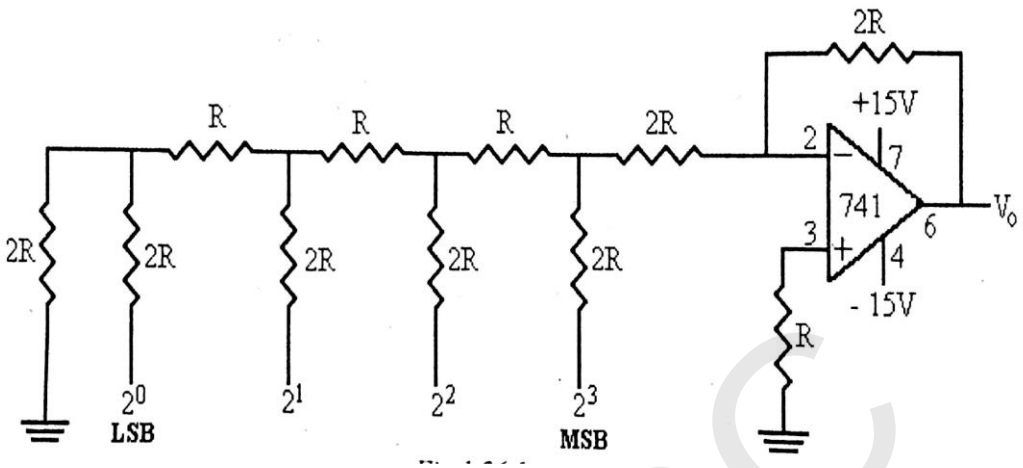
VCO is used in FM, FSK, and tone generators, where the frequency needs to be controlled by means of an input voltage called control voltage.

4. What is PLL?

PLL is a control system that generates an output signal whose phase is related to the phase of input Reference signal.

CIRCCUIT DIAGRAMS:

DAC:

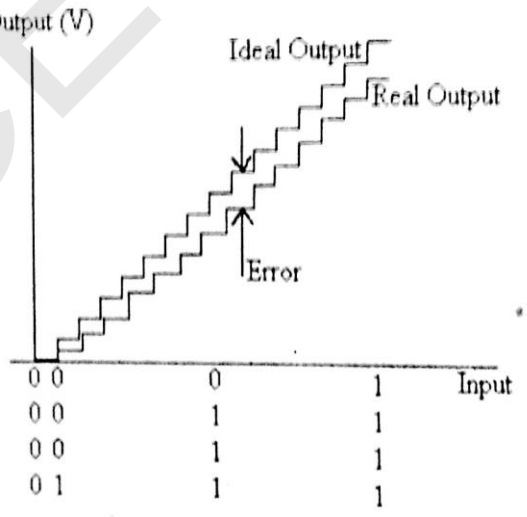


Observations:

$Q_3Q_2Q_1Q_0$	V_O (Volts)
0000	
0001	
0010	
.....	
.....	
1101	
1110	
1111	

Table 1.26.1

Typical Response Curve:



Exp No: 13 **Date:**

D/A CONVERTER R-2R LADDER NETWORK

AIM:

To design set up a R-2R ladder type DAC.

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	1.5KΩ(2),1MΩ,4.7KΩ(pot),220Ω (2)	Each one
5	Capacitors	0.1Uf	3
6	Diode	IN 4007	1
7	Op-amp	IC 741	1
8	LED		2
9	Bread board	-	1
10	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

R-2R ladder type DAC: It uses resistor of only two values R and2R.The inputs to resistor network may be applied through digitally connected switches or from output pins of a counter. The analogue output will be maximum, when all inputs are of logic high.
V=-Rf/R (Q3/2 + Q2/4+ Q1/8+ Q0/16). Where each input Q3, Q2, Q1 and Q0 may be high (+5V) or low (0V).

PROCEDURE:
1. Verify the conditions of op-amp.
2. Set up the DAC circuit and manually enter binary inputs 0000 to 1111.
3. Measure the output voltage using a multimeter and tabulate the readings.
4. Draw the response with analog output on Y-axis and binary output on X-axis.

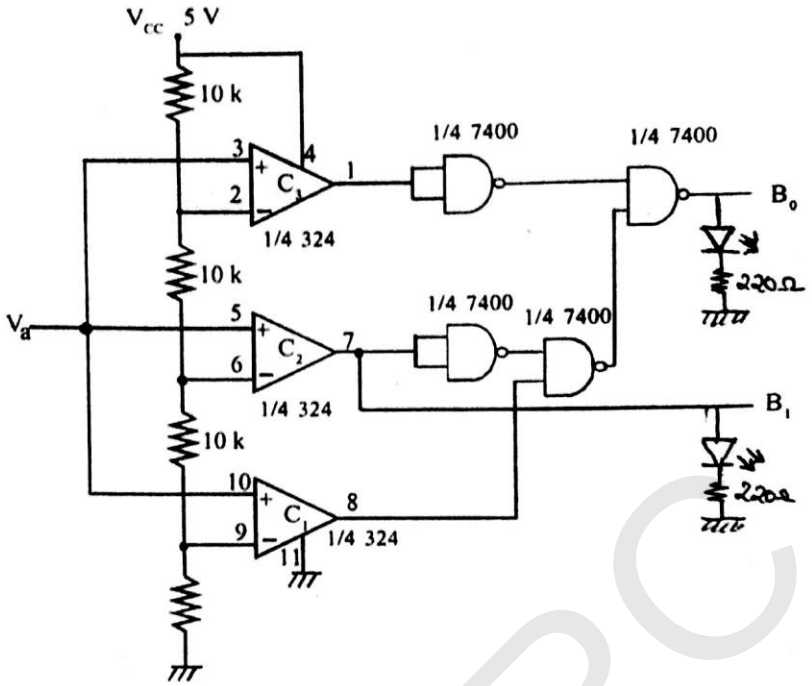
RESULT:

Designed and Studied DAC

INFERENCE:

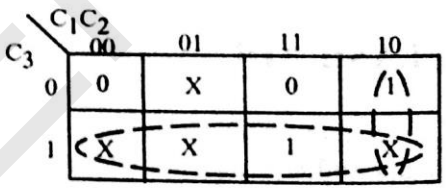
DAC
Analog output equivalent to the digital input 0010 =…….
Analog output equivalent to the digital input 1010 =……
ADC:

Circuit diagram



Design

Comparator o/p			Binary o/p	
C_1	C_2	C_3	B_1	B_0
0	0	0	0	0
1	0	0	0	1
1	1	0	1	0
1	1	1	1	1



$B_0 = C_1 + C_1\overline{C}_2$

From direct inspection of truth table, we get, $B_1 = C_2$

Exp No: 14 **Date:**

A/D CONVERTER FLASH TYPE

AIM:

To design set up a flash type ADC.

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	1.5KΩ(2),1MΩ,4.7KΩ(pot),220Ω(2)	Each one
5	Capacitors	0.1Uf	3
6	Diode	IN 4007	1
7	Op-amp	IC 741	1
8	LED		2
9	Bread board	-	1
10	Connecting wires	-	As required

PRINCIPLE & PROCEDURE:

2-bit flash ADC: If the analog signal exceeds the reference signal to any comparator, that comparator turns on. If all comparators are off, analog input will be between 0 and +V/4. If C1 is high and C2 and C3 are low, input will be between +V/4 and +V/2. If C1 and C2 are high and C3 is low input will be between +V/2 and +3V/4. If all comparators are high, analog input will be between +3V/4 and +V. the outputs of three comparators are then fed to a coding network to provide 2 bits which are equivalent to the input analog voltage.

PROCEDURE:

1. Verify the conditions of op-amp.
2. Set up the circuit for ADC including the encoder network.
3. Vary the analog input from 0 to 5V and observe the output bits

RESULT:

Designed and studied DAC and ADC circuits.

INFERENCE:

ADC

Digital output equivalent to the analog input 0 - 1.25V =…….

Digital output equivalent to the analog input 1.25 – 2.5V =…….

Digital output equivalent to the analog input 2.5 - 3.75V =…….

Digital output equivalent to the analog input 3.75 – 5V =……

VIVA QUESTIONS:

1. **List all the types of DAC.**

   a) Weighted resistor
   b) R-2R ladder
   c) Inverted R-2R ladder.

2. **What is the advantage of R-2R ladder over weighted resistor?**

In weighted resistor, for higher order conversion the values of resistors become very high which is overcome in R-2R ladder which has only R and 2R values of resistors.

3. **List the various types of ADC**.

   i) Direct type
      a) Flash type
      b) Counter
      c) Successive Approximation Register
      d) Tracking

   ii) Integrating type
      a) Charge balancing
      b) Integrating

4. **Define resolution.**

   Smallest change in voltage which may be produced at output of the converter.

5. **List the specifications of DAC and ADC.**

   a) Resolution
   b) Linearity
   c) Accuracy
   d) Monotonicity
   e) Settling time
   f) Stability.

6. **The basic step of 9 bit DAC is 10.3mV. If 000000000 represents 0V. What output is produced if the input is 101101111?**

   7.38mV.

7. **State the applications of DAC and ADC .**

   a) Digital signal processing
   b) Communication circuits

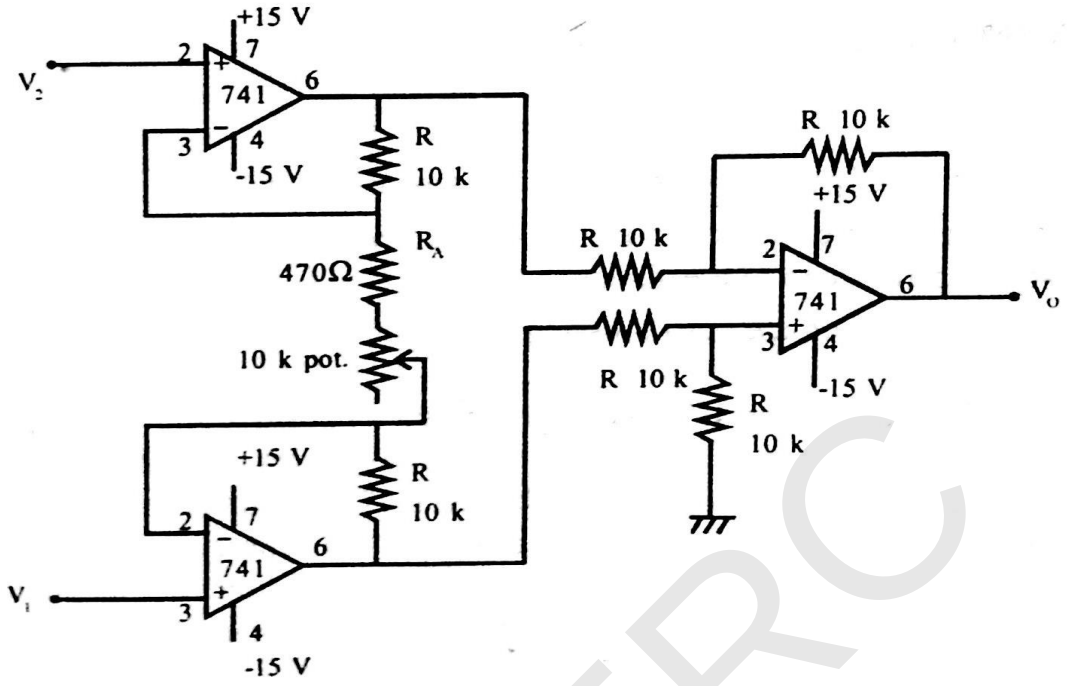
8. **For R-2R ladder 4 bit type DAC find the output voltage if digital input is 1111. Assume VR = 10V, R = Rf = 10K.**

Vo = 9.375V

9. Which is the fastest type of ADC? Why?

Successive approximation is the fastest type of ADC. It completes n-bit conversion in n clock periods.

CIRCUIT DIAGRAM:



Design We have, $V_O = (V_1 - V_2)[1 + 2R/R_A max]$

Given, $1 + 2R/R_A max = 3$

Take R and R_A = 10 k. Use 10 k pot in series with 470 Ω.

Exp No: 15 **Date:**

INSTRUMENTATION AMPLIFIER

AIM:

To design and set up an instrumentation amplifier using three op-amps to obtain minimum gain of 3 for difference of inputs.

APPARATUS REQUIRED:

The following components and equipments are used for conducting the experiment.

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V Variable power supply	1 2
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	10KΩ(6),470Ω,10KΩ(pot)	Each one
5	Op-amp	IC 741	3
6	Bread board	-	1
7	Connecting wires	-	As required

PRINCIPLE:

Instrumentation amplifiers are widely used in data acquisition systems, remote sensing applications and instrumentation systems to measure temperature, humidity, light intensity and weight etc. Most of the instrumentation systems use a transducer in a bridge circuit. Instrumentation amplifier facilitates the amplification of potential difference take place due to the imbalance of the bridge circuit proportional to a change in physical quantity. The main feature of instrumentation amplifiers are high gain, high input resistance, high CMRR etc.

PROCEDURE:

1.Verify the condition of op-amps.
2.Setup V_1 =0.5V dc and V_2 =0.4V dc and measure output voltage on CRO or using multimeter, keeping Ra in maximum position.
3. Repeat the step2 by keeping Ra in minimum position. Note down the increase in gain. This is the difference mode gain A_d.
4. Feed V_1= V_2= 0.5V and observe the gain keeping R_a in minimum positon this is common mode gain A_c.Calculate CMRR from the relation CMRR= 20 log (A_d / A_c).

RESULT:

Designed and studied instrumentation amplifier.

INFERENCE:

CMRR =……..

VIVA QUESTIONS:

1. **What is the need for an instrumentation amplifier?**

   In a number of industrial and consumer applications, the measurement of physical quantities is usually done with the help of transducers.

2. **Mention some of the linear applications of op – amps.**

   Adder, subtractor, voltage to current converter, current to voltage converters, instrumentation amplifier, analog computation, power amplifier, etc are some of the linear op-amp circuits.

3. **Mention some of the non – linear applications of op-amps.**

   Rectifier, peak detector, clipper,clamper, sample and hold circuit, log amplifier anti–log amplifier, multiplier are some of the non – linear op-amp circuits.

4. **What are the areas of application of non-linear op- amp circuits?**

   Industrial instrumentation, Communication and Signal processing.

CIRCUIT DIAGRAMS:

Log Amplifier using Diode

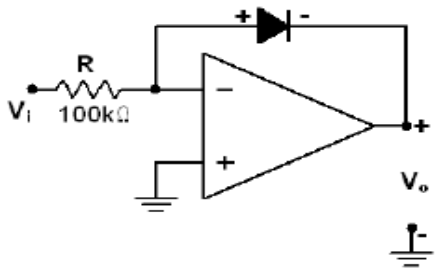


Fig 1

Log Amplifier Using a BJT

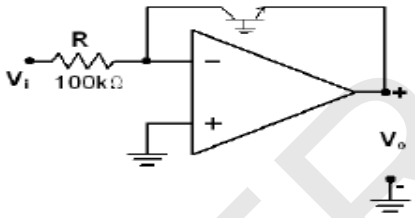


Fig 2

Anti-log Amplifier

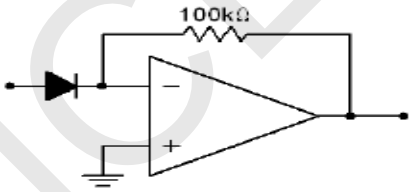


Fig 3

Log - Antilog Amplifier

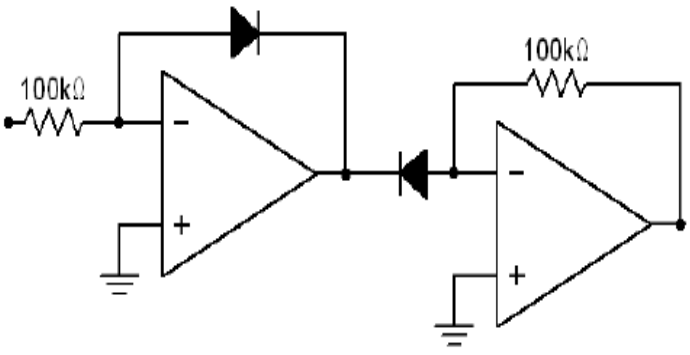


Fig 4

Exp No:16 **Date:**

LOG AND ANTILOG AMPLIFIERS

AIM:

To understand the behavior of logarithmic and antilogarithmic amplifiers.

APPARATUS REQUIRED:

The following components and equipments are used for log and antilog amplifiers

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	100KΩ	2
5	Multimeter		1
6	Diode	IN 4007	2
7	Op-amp	IC 741	2
8	Bread board	-	1
9	Connecting wires	-	As required

PRINCIPLE:

Log amplifiers are widely used for analog signal compression applications. When a diode used in the feedback loop of an operational amplifier is forward biased by a constant current of magnitude V_i /R then it develops a potential

$$V_D = V_T \ln\left(\frac{v_i}{RI_o}\right)$$

across the diode. Note that the input voltage and diode voltage are related in a logarithmic fashion. If we take the diode voltage as an output voltage then the input and output will be related in a logarithmic fashion. The base emitter junction of a bipolar junction transistor can be used as diode when collector and base are shorted. So a transistor can also be used in the feedback loop of an op-amp. Antilog is inverse operation of log operation so; antilog amplifiers can be designed by reversing the arrangement of diodes and resistors in the log amplifiers. It is important to note that a single polarity of current can only forward bias the diode. That means the log operation or antilog operation is single quadrant operation.

PROCEDURE:

Log amplifier:

1. Set up the circuit for log amplifier using diode and transistor.
2.Set the input voltage to 1V.and see the voltage across the diode and voltage across the output terminal. Note the negative sign.
4. Increase the input voltage in the step of 1V up to 20V.
5. Plot the characteristics of input voltage and output voltage.

6. Compare the characteristics of diode based log amplifier with that of transistor based log amplifier.
7. Reverse the polarity of the diode and see the effect for positive input voltage.

Anti log amplifier:

1. Set up the circuit for antilog amplifier using diode. Set the input voltage to 100mV.
2. See the voltage across the Resistor. Note the negative sign.
3. Increase the input voltage in the step of 50mV up to 500mV.
4. Plot the characteristics of input voltage and output voltage.
5. Reverse the polarity of the diode and see the effect for positive input voltage.

Log-anti log amplifier:

1Set up the circuit for log-antilog amplifier
2 Set the input voltage to 1V.See the voltage across the output resistor.
3 Increase the input voltage in the step of 1V up to 20V.
4 Note the output voltage for all the input voltages.
5 Please get confused why the output is not the exact replica of input.
6 Reverse the polarity of diode in the antilog amplifier of fig 4.
7Again set the input to 1V.
8 See the output and be angry with the output.
9 Increase the input from 1V and see the output.

RESULT:

Studied log and antilog amplifiers.

INFERENCE:

VIVA QUESTIONS:

1. **What is sample and hold circuit?**

   A sample and hold circuit samples an input signal and holds on to its last sampled value until the input sampled again.

2. **What is the application of sample and hold circuit?**

   Digital interfacing, ADC, pulse code modulation system.

3. **What is the application of logarithmic amplifier?**

   Calculator, computer.

4. **What is the function of a diode in a feedback loop in a logarithmic amplifier?**

   In logarithmic amplifier circuit, diode acts as clipper.

5. **What is the use of resistor R in clamper?**

   The resistor R is used to protect the Op-amp. against excessive discharge current from capacitor especially when the DC supply voltages are switched off.

APPENDIX

STUDY OF OP AMPS - IC 741, IC 555, IC 565, IC 566 AND VOLTAGE REGULATOR IC 723

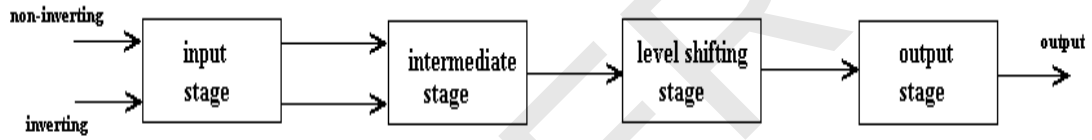
FUNCTIONING, PARAMETERS AND SPECIFICATIONS

IC 741 :

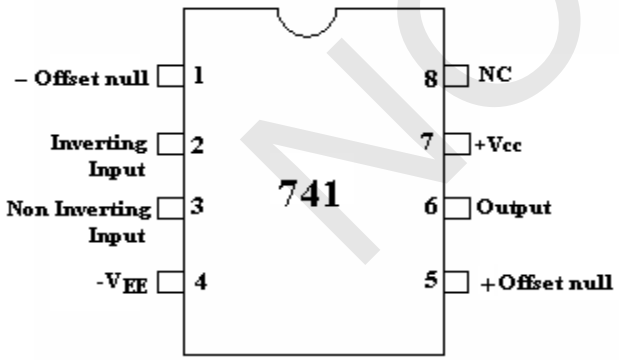
General Description:

The IC 741 is a high performance monolithic operational amplifier constructed using the planer epitaxial process. High common mode voltage range and absence of latch-up tendencies make the IC 741 ideal for use as voltage follower. The high gain and wide range of operating voltage provide superior performance in integrator, summing amplifier and general feedback applications.

Block Diagram of Op-Amp:



Pin Configuration:



Features:

1. No frequency compensation required.
2. Short circuit protection
3. Offset voltage null capability
4. Large common mode and differential voltage ranges
5. Low power consumption
6. No latch-up

Specifications:

1. Voltage gain A = α typically 2,00,000
2. I/P resistance R_L = α Ω, practically 2MΩ
3. O/P resistance R =0, practically 75Ω
4. Bandwidth = α Hz. It can be operated at any frequency

5. Common mode rejection ratio = α
   (Ability of op amp to reject noise voltage)
6. Slew rate + α V/μsec
   (Rate of change of O/P voltage)
7. When $V_1 = V_2$, V_D=0
8. Input offset voltage (Rs ≤ 10KΩ) max 6 mv
9. Input offset current = max 200nA
10. Input bias current : 500nA
11. Input capacitance : typical value 1.4pF
12. Offset voltage adjustment range : ± 15mV
13. Input voltage range : ± 13V
14. Supply voltage rejection ratio : 150 μV/V
15. Output voltage swing: + 13V and – 13V for R_L > 2KΩ
16. Output short-circuit current: 25mA
17. supply current: 28mA
18. Power consumption: 85mW
19. Transient response: rise time= 0.3 μs, Overshoot= 5%

Applications:

1. AC and DC amplifiers
2. Active filters
3. Oscillators
4. Comparators
5. Regulators

IC 555:

Description:

The operation of SE/NE 555 timer directly depends on its internal function. The three equal resistors R_1, R_2, R_3 serve as internal voltage divider for the source voltage. Thus one-third of the source voltage V_{CC} appears across each resistor.

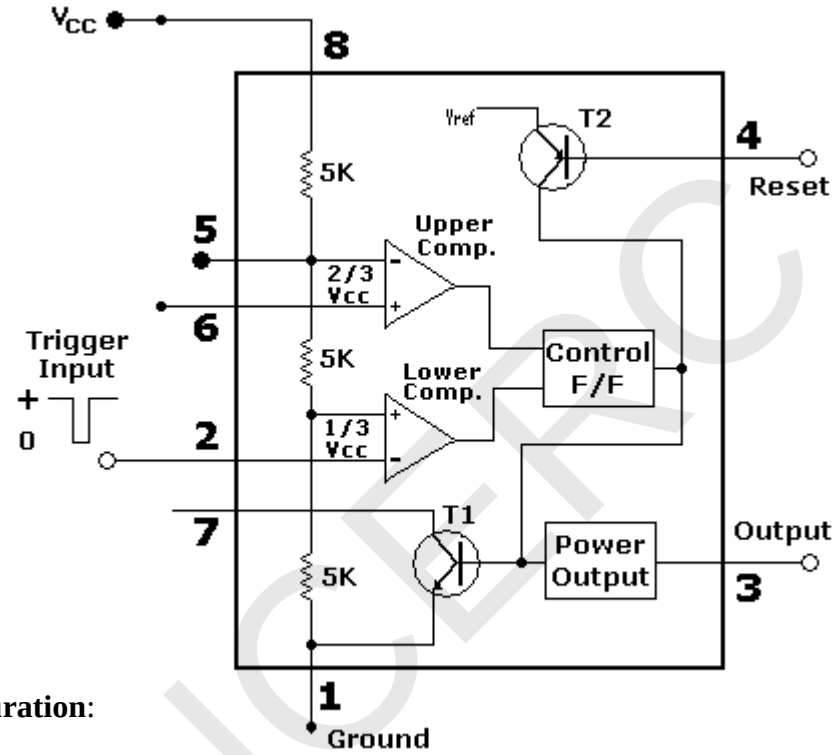
Comparator is basically an Op amp which changes state when one of its inputs exceeds the reference voltage. The reference voltage for the lower comparator is +1/3 V_{CC}. If a trigger pulse applied at the negative input of this comparator drops below +1/3 V_{CC}, it causes a change in state. The upper comparator is referenced at voltage +2/3 V_{CC}. The output of each comparator is fed to the input terminals of a flip flop.

The flip-flop used in the SE/NE 555 timer IC is a bistable multivibrator. This flip flop changes states according to the voltage value of its input. Thus if the voltage at the threshold terminal rises above +2/3 V_{CC}, it causes upper comparator to cause flip-flop to change its states. On the other hand, if the trigger voltage falls below +1/3 V_{CC}, it causes lower comparator to change its states. Thus the output of the flip flop is controlled by the voltages of the two comparators. A change in state occurs when the threshold voltage rises above +2/3 V_{CC} or when the trigger voltage drops below +1/3 V_{cc}.

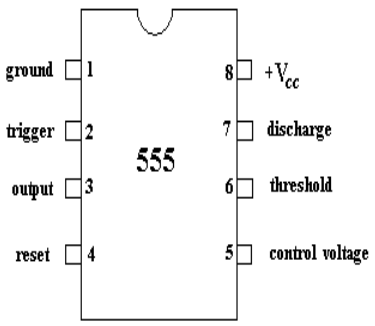
The output of the flip-flop is used to drive the discharge transistor and the output stage. A high or positive flip-flop output turns on both the discharge transistor and the output stage. The discharge transistor becomes conductive and behaves as a low resistance short circuit to ground. The output stage behaves similarly. When the

flip-flop output assumes the low or zero states reverse action takes place i.e., the discharge transistor behaves as an open circuit or positive V_{CC} state. Thus the operational state of the discharge transistor and the output stage depends on the voltage applied to the threshold and the trigger input terminals.

Block Diagram of IC 555:



Pin Configuration:



Function of Various Pins of 555 IC:

Pin (1) of 555 is the ground terminal; all the voltages are measured with respect to this pin.

Pin (2) of 555 is the trigger terminal, If the voltage at this terminal is held greater than one-third of V_{CC}, the output remains low. A negative going pulse from V_{cc} to less

than $V_{ec}/3$ triggers the output to go High. The amplitude of the pulse should be able to make the comparator (inside the IC) change its state. However the width of the negative going pulse must not be greater than the width of the expected output pulse.

Pin (3) is the output terminal of IC 555. There are 2 possible output states. In the low output state, the output resistance appearing at pin (3) is very low (approximately 10 Ω). As a result the output current will goes to zero , if the load is connected from Pin (3) to ground , sink a current I_{Sink} (depending upon load) if the load is connected from Pin (3) to ground, and sinks zero current if the load is connected between $+V_{CC}$ and Pin (3).

Pin (4) is the Reset terminal. When unused it is connected to $+V_{cc}$. Whenever the potential of Pin (4) is drives below 0.4V, the output is immediately forced to low state. The reset terminal enables the timer over-ride command signals at Pin (2) of the IC.

Pin (5) is the Control Voltage terminal.This can be used to alter the reference levels at which the time comparators change state. A resistor connected from Pin (5) to ground can do the job. Normally 0.01μF capacitor is connected from Pin (5) to ground. This capacitor bypasses supply noise and does not allow it affect the threshold voltages.

Pin (6) is the threshold terminal. In both astable as well as monostable modes, a capacitor is connected from Pin (6) to ground. Pin (6) monitors the voltage across the capacitor when it charges from the supply and forces the already high O/p to Low when the capacitor reaches $+2/3\ V_{CC}$.

Pin (7) is the discharge terminal. It presents an almost open circuit when the output is high and allows the capacitor charge from the supply through an external resistor and presents an almost short circuit when the output is low.

Pin (8) is the $+V_{cc}$ terminal. 555 can operate at any supply voltage from +3 to +18V.

Features of 555 IC

1. The load can be connected to o/p in two ways i.e. between pin 3 & ground 1 or between pin 3 & V_{CC} (supply)
2. 555 can be reset by applying negative pulse, otherwise reset can be connected to $+V_{cc}$ to avoid false triggering.
3. An external voltage effects threshold and trigger voltages.
4. Timing from micro seconds through hours.
5. Monostable and bistable operation
6. Adjustable duty cycle
7. Output compatible with CMOS, DTL, TTL
8. High current output sink or source 200mA
9. High temperature stability
10. Trigger and reset inputs are logic compatible.

Specifications:

1.	Operating temperature	:	SE 555-- -55°C to 125°C NE 555-- 0° to 70°C
2.	Supply voltage	:	+5V to +18V
3.	Timing	:	μSec to Hours
4.	Sink current	:	200mA
5.	Temperature stability	:	50 PPM/°C change in temp or 0-005% /°C.

Applications:

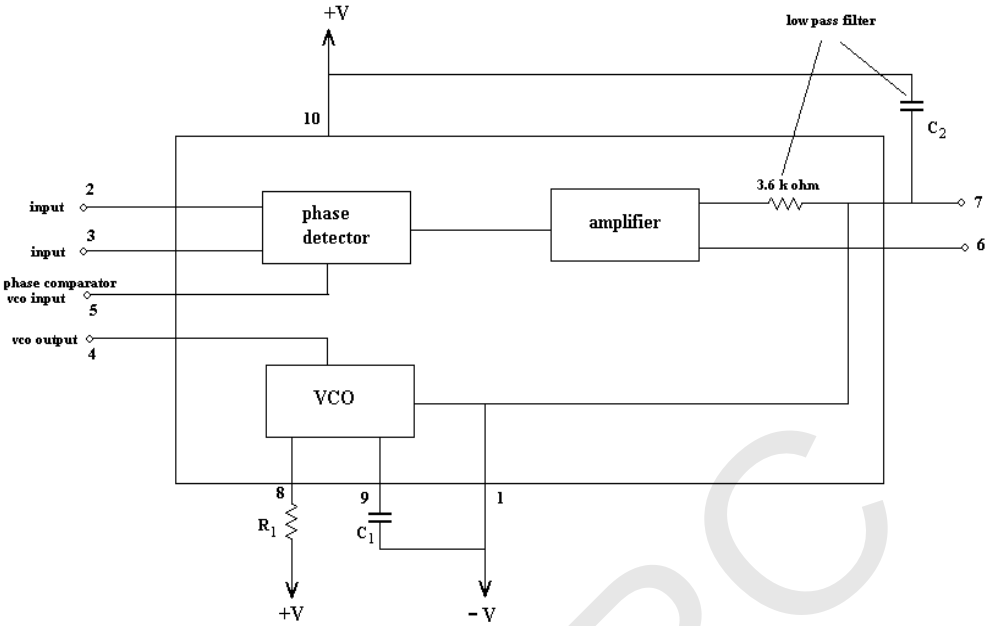
1. Monostable and Astable Multivibrators
2. dc-ac converters
3. Digital logic probes
4. Waveform generators
5. Analog frequency meters
6. Tachometers
7. Temperature measurement and control
8. Infrared transmitters
9. Regulator & Taxi gas alarms etc

IC 565:

Description:

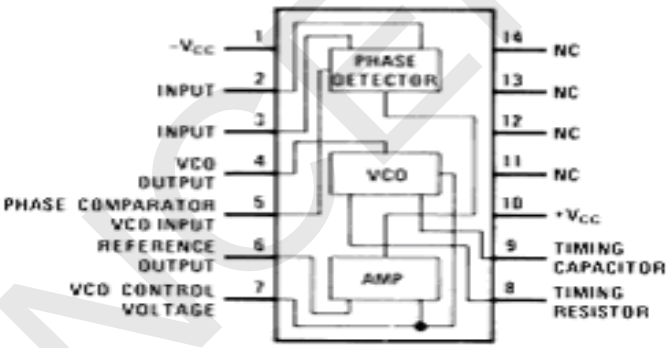
The Signetics SE/NE 560 series is monolithic phase locked loops. The SE/NE 560, 561, 562, 564, 565, & 567 differ mainly in operating frequency range, power supply requirements and frequency and bandwidth adjustment ranges. The device is available as 14 Pin DIP package and as 10-pin metal can package. Phase comparator or phase detector compare the frequency of input signal f_s with frequency of VCO output f_o and it generates a signal which is function of difference between the phase of input signal and phase of feedback signal which is basically a d.c voltage mixed with high frequency noise. LPF remove high frequency noise voltage. Output is error voltage. If control voltage of VCO is 0, then frequency is center frequency (f_o) and mode is free running mode. Application of control voltage shifts the output frequency of VCO from f_o to f. On application of error voltage, difference between f_s & f tends to decrease and VCO is said to be locked. While in locked condition, the PLL tracks the changes of frequency of input signal.

Block Diagram of IC



565

Pin Configuration:



Specifications:

1. Operating frequency range : 0.001 Hz to 500 KHz
2. Operating voltage range : ±6 to ±12V
3. Inputs level required for tracking : 10mV rms minimum to 3v (p-p) max.
4. Input impedance : 10 KΩ typically
5. Output sink current : 1mA typically
6. Drift in VCO center frequency (f_{out}) with temperature : 300 PPM/^oC typically
7. Drif in VCO centre frequency with supply voltage : 1.5%/V maximum
8. Triangle wave amplitude : typically 2.4 V_{PP} at ± 6V
9. Square wave amplitude : typically 5.4 V_{PP} at ± 6V
10. Output source current : 10mA typically
11. Bandwidth adjustment range : <±1 to >± 60%

Center frequency $f_{out} = 1.2/4R_1C_1$ Hz

= free running frequency

$F_L = \pm 8\ f_{out}/V$ Hz

$V = (+V) - (-V)$

$$f_c = \pm \left[\frac{f_L}{2\Pi(3.6)x10^3 xC2} \right]^{1/2}$$

Applications:

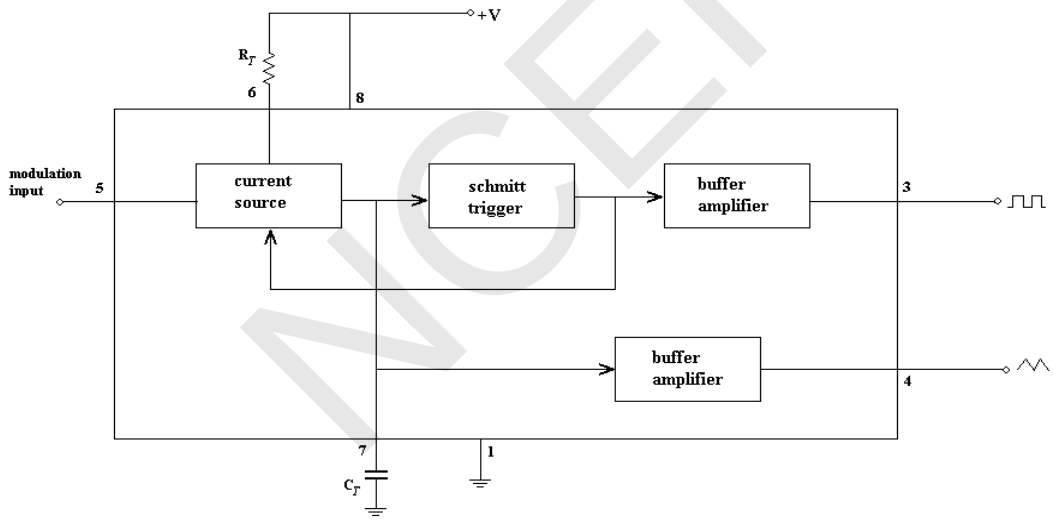
1. Frequency multiplier
2. Frequency shift keying (FSK) demodulator
3. FM detector

IC 566:

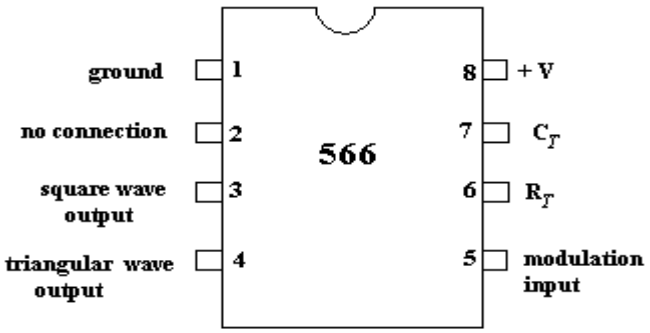
Description:

The NE/SE 566 Function Generator is a voltage controlled oscillator of exceptional linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage with exceptional linearity.

Block Diagram of IC566



Pin diagram:



Specifications:

Maximum operating Voltage --- 26V

Input voltage --- 3V (P-P)

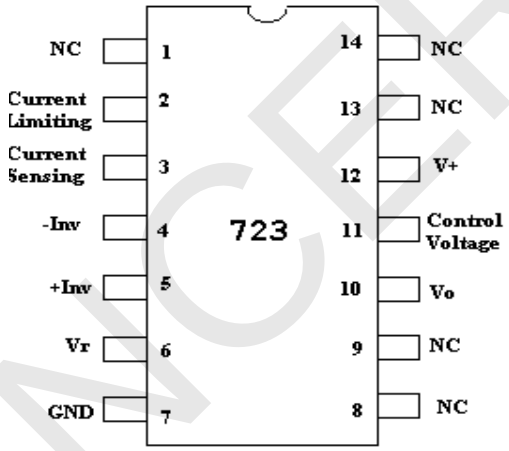
Storage Temperature	---	-65°C to + 150°C
Operating temperature	---	0°C to +70°C for NE 566 -55°C to +125°C for SE 566
Power dissipation	---	300mv

Applications:

1. Tone generators.
2. Frequency shift keying
3. FM Modulators
4. clock generators
5. signal generators
6. Function generator

IC723

Pin Configuration



Specifications of 723:

Power dissipation	:	1W
Input Voltage	:	9.5 to 40V
Output Voltage	:	2 to 37V
Output Current	:	150mA for Vin-Vo = 3V 10mA for Vin-Vo = 38V
Load regulation	:	0.6% Vo
Line regulation	:	0.5% Vo

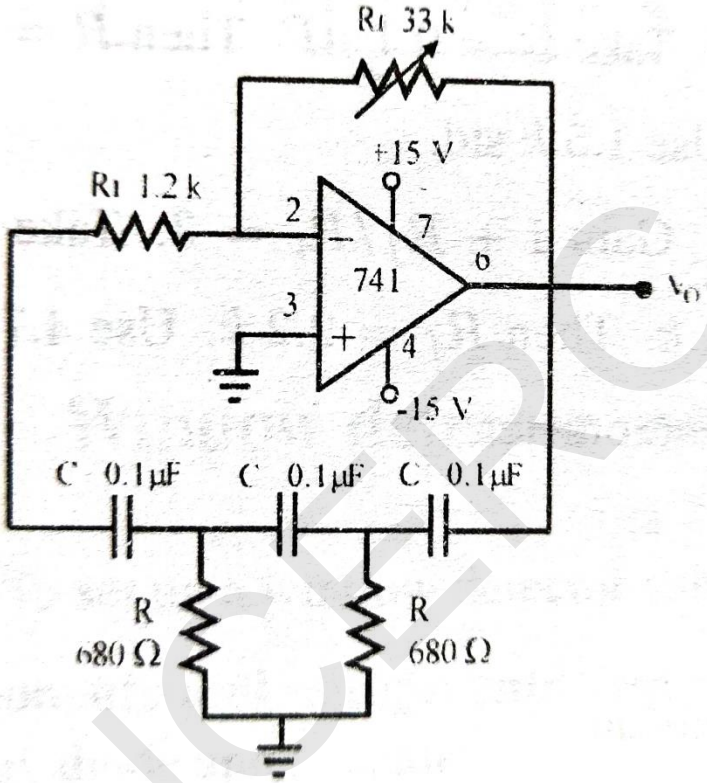
Design:

Let the required frequency f_0 be $\frac{1}{2\pi\sqrt{6RC}} = 1kHz$

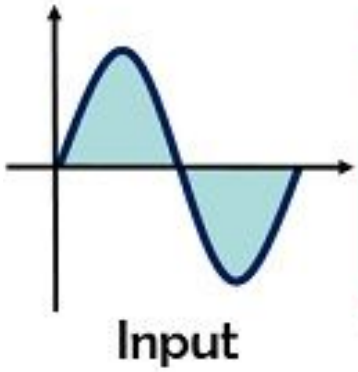
Take C=0.1μF. Then R= 650Ω. Use 680Ω

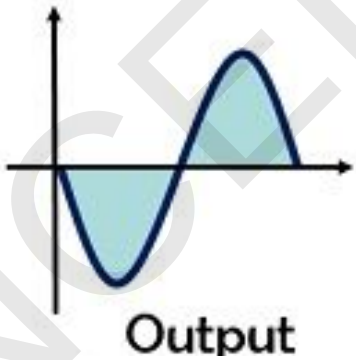
Gain $R_f/R_i = 29$. Take R_i = 1.2k and R_f = 33k pot

Circuit Diagram:



Model Graph:





180^0 phase shift

Exp No: 17 **Date:**

RC PHASE SHIFT OSCILLATOR

AIM:

To design and setup an RC phase shift oscillator using op-amp for a frequency of 1 kHz.

APPARATUS REQUIRED:

The following components and equipment's are used to design and set up a RC phase shift Oscillator

S.No	DESCRIPTION	RANGE	QUANTITY
1	Power Supply	15 V	1
2	Function generator	1MHz	1
3	CRO		1
4	Resistors	680Ω 1.2k 33k pot	2 1 1
5	Capacitors	0.1µF	3
6	Op-amp	IC 741	1
7	Bread board	-	1
8	Connecting wires	-	As required

PRINCIPLE:

RC phase shift oscillator consists an op-amp as the amplifying stage and three RC cascaded networks as the feedback network. The feedback network provides a fraction of the output voltage back to the input of the amplifier. The op-amp is functioning in the inverting mode. Therefore, any signal which appears at the inverting terminal is shifted by 180^o at the output. An additional 180^o phase shift

required for oscillation as per Barkhausen criteria, is provided by the cascaded RC network. Thus, the total phase shift around the loop becomes 0^o.

The frequency of oscillation is given by,

$$f_0 = \frac{1}{2\pi\sqrt{6RC}}$$

The gain of the inverting op amp should be at least 29 at this frequency because that attenuation provided by the feedback network is 1/29. The gain is kept slightly greater than 29 to ensure that the variations in circuit parameters will not make the loop gain less than unity, and thus oscillations die out. For lower frequencies (< 1MHz), op amp 741 may be used, however for high frequencies LM318 or LF351 should be used.

PROCEDURE:

1. Verify whether the op-amp is in good condition and set up the circuit as shown in the circuit diagram.
2. Note down the amplitude and frequency of output waveform.

RESULT:

Designed and Studied RC phase shift oscillator circuit and the waveform was observed on CRO.

Exp No: 18 **Date:**

PRECISION RECTIFIERS USING OP-AMPS

AIM:

To study the Half Wave and Full Wave Rectifier and to obtain the required graph

APPARATUS REQUIRED:

Sl.No.	Equipment and Components	Range / Number/ Value	Qty
1	Integrated Regulated Power Supply (ICPS)	±15 V	1
2	Cathode Ray Oscilloscope (CRO)	20 / 40MHz, Dual Trace	1
3	Function Generator	1 MHz	1
4	Operational Amplifier (OP-AMP)	IC 741	1
5	Resistor	10kΩ , 4.7k, 2.7k	5+2
6	Diode	1N 4007	2
7	Bread board & Connecting wires		

THEORY:

An inverting Op-Amp can be converted into a half wave rectifier by adding two diodes. When V_i is positive, diode D_1 conducts causing V_o to go to positive by one diode drop. Hence diode D_2 is reverse biased. The output voltage V_o is zero because for all practical purposes no current flows through D_1 for –ve input, D_2 conducts and D_1 is OFF. The – ve input V_i forces the Op-Amp output V_o –ve and causes D_2 to conduct. The circuit then acts like inverter for $R_f = R_1$ and the output V_o becomes positive. The Op-Amp in the circuit must be high Op-Amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the Op-Amp. As the input passes through zero the Op-Amp output V_o must change from 0.6 to -0.6v or vice versa as quickly as possible in order to switch over the conduction from one diode to another

PROCEDURE:

1.Connections are made as per the circuit diagram
2.A sinusoidal signal from audio oscillator is applied to the inverting terminal of op-*amp
3.The rectified output is then obtained on the CRO

RESULT:

The Half Wave and Full Wave Precision rectifier is constructed and output is obtained.

HALF WAVE RECTIFIER

CIRCUIT DIAGRAM:

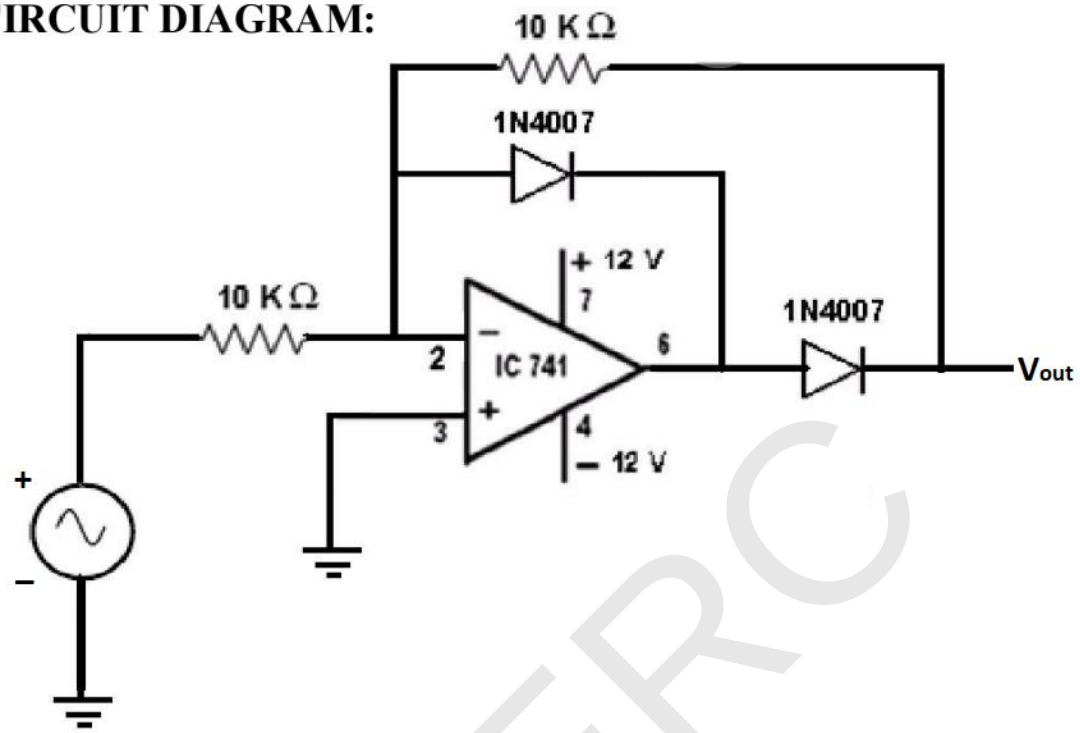
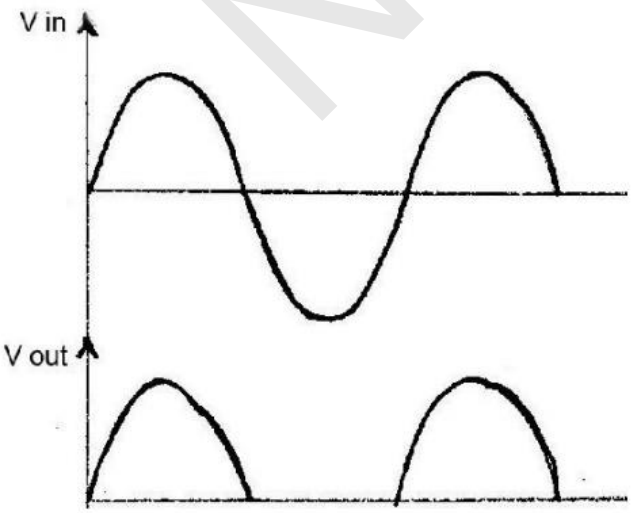


Fig: Half Wave Rectifier

MODEL GRAPH



FULL WAVE RECTIFIER

CIRCUIT DIAGRAM

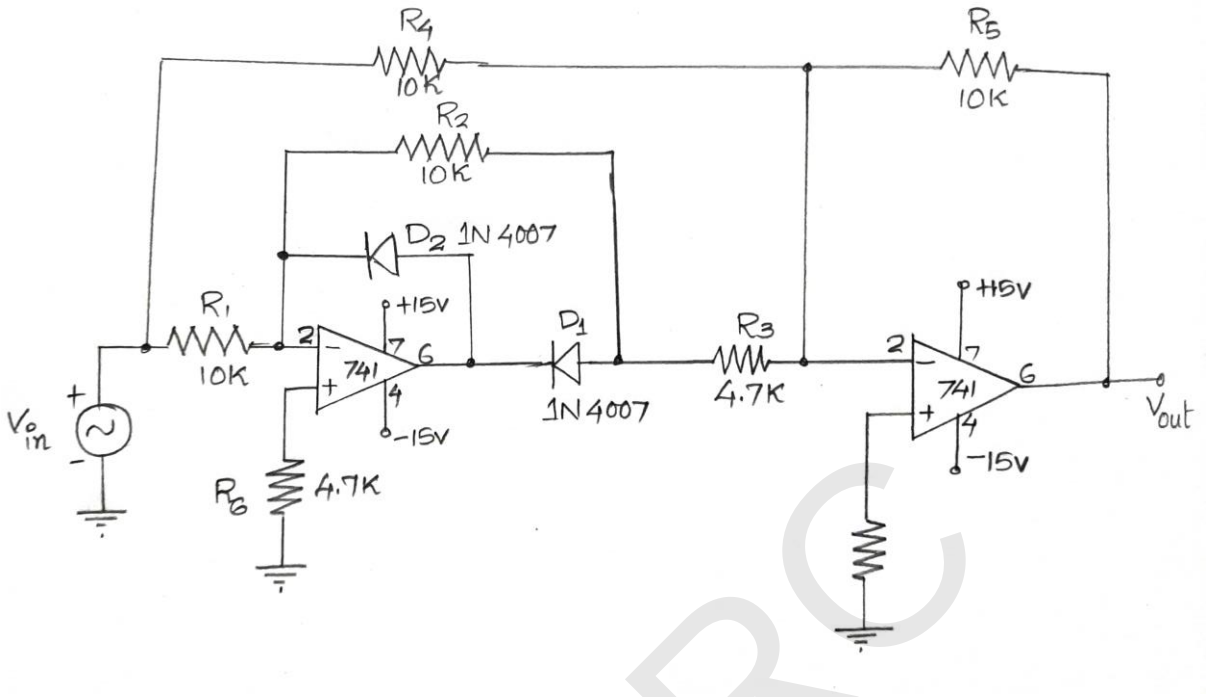
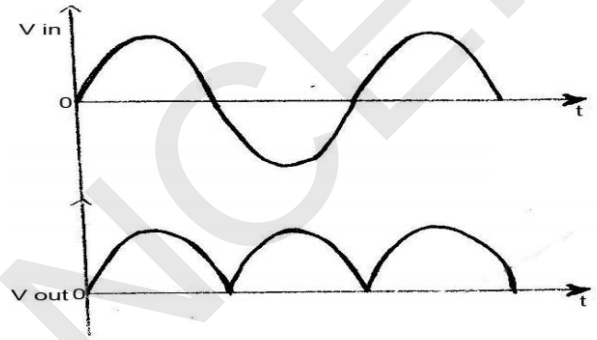


Fig: Full Wave Rectifier

MODEL GRAPH



TABULATION:

Sl.No.	Description	Input		Output	
		Amplitude	Time	Amplitude	Time
1	Half Wave				
2	Full Wave				

Exp No: 19 **Date:**

SIMULATION OF RC PHASE SHIFT OSCILLATOR USING PSPICE

AIM:

To simulate the RC Phase shift Oscillator using op-amp to generate the sinewave.

SOFTWARE REQUIRED:

OrCAD software.

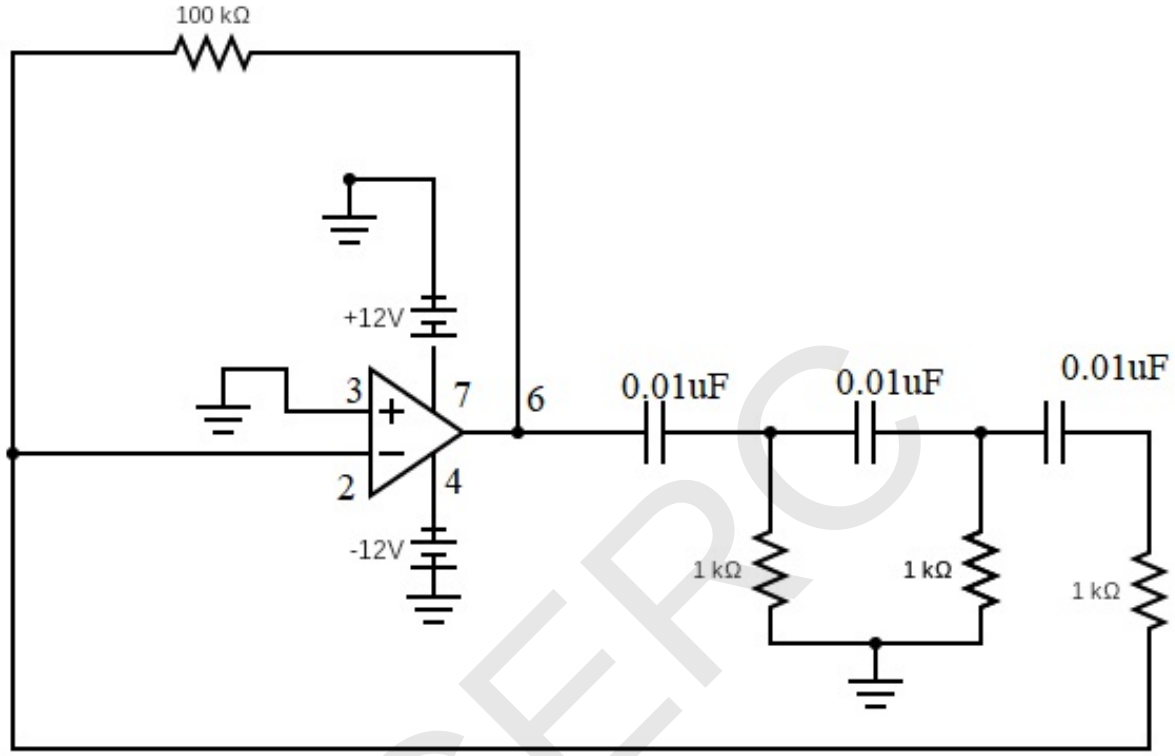
PROCEDURE:

- Switch on the computer and select ORCAD PSPICE ion.
- Open a new project to design a circuit in the file menu.
- Select the required components from the library.
- Draw the circuit as shown in figure tool bar.
- After completing save the project and go to simulation tool bar
- Verify the simulated output and take a print out.

RESULT:

Thus the RC Phase Shift Oscillator using op-amp using PSPICE was simulated and tested.

CIRCUIT DIAGRAM (RC PHASE SHIFT OSCILLATOR)



Exp No:20 **Date:**

SIMULATION OF WEIN BRIDGE OSCILLATOR USING PSPICE

AIM:

To simulate the Wein Bridge Oscillators using op-amp to generate sinewave.

SOFTWARE REQUIRED:

OrCAD software.

PROCEDURE:

- Switch on the computer and select ORCAD PSPICE ion.
- Open a new project to design a circuit in the file menu.
- Select the required components from the library.
- Draw the circuit as shown in figure tool bar.
- After completing save the project and go to simulation tool bar
- Verify the simulated output and take a print out.

RESULT:

Thus, the Wein Bridge Oscillators using op-amp using PSPICE was simulated and tested.

CIRCUIT DIAGRAM (WEIN BRIDGE OSCILLATOR)